 <i>Good Display</i>	E paper IC Specifications	SPEC NO	
	IL0373	REV NO	

# Good Display Specifications

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Issue Date: 2016.4.7



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## INTRODUCTION

This driver is an all-in-one driver with timing controller for ESL. Its output is of 1-bit white/black and 1-bit red resolution per pixel. The timing controller provides control signals for the source driver and gate drivers.

The DC-DC controller allows it to generate the source output voltage  $V_{DH}/V_{DL}$  ( $\pm 2.4V \sim \pm 11V$ ). The chip also includes an output buffer for the supply of the COM electrode ( $V_{COMAC}$  or  $V_{COMDC}$ ). The system is configurable through a 3-wire/4-wire (SPI) serial interface.

## MAIN APPLICATIONS

- E-tag application

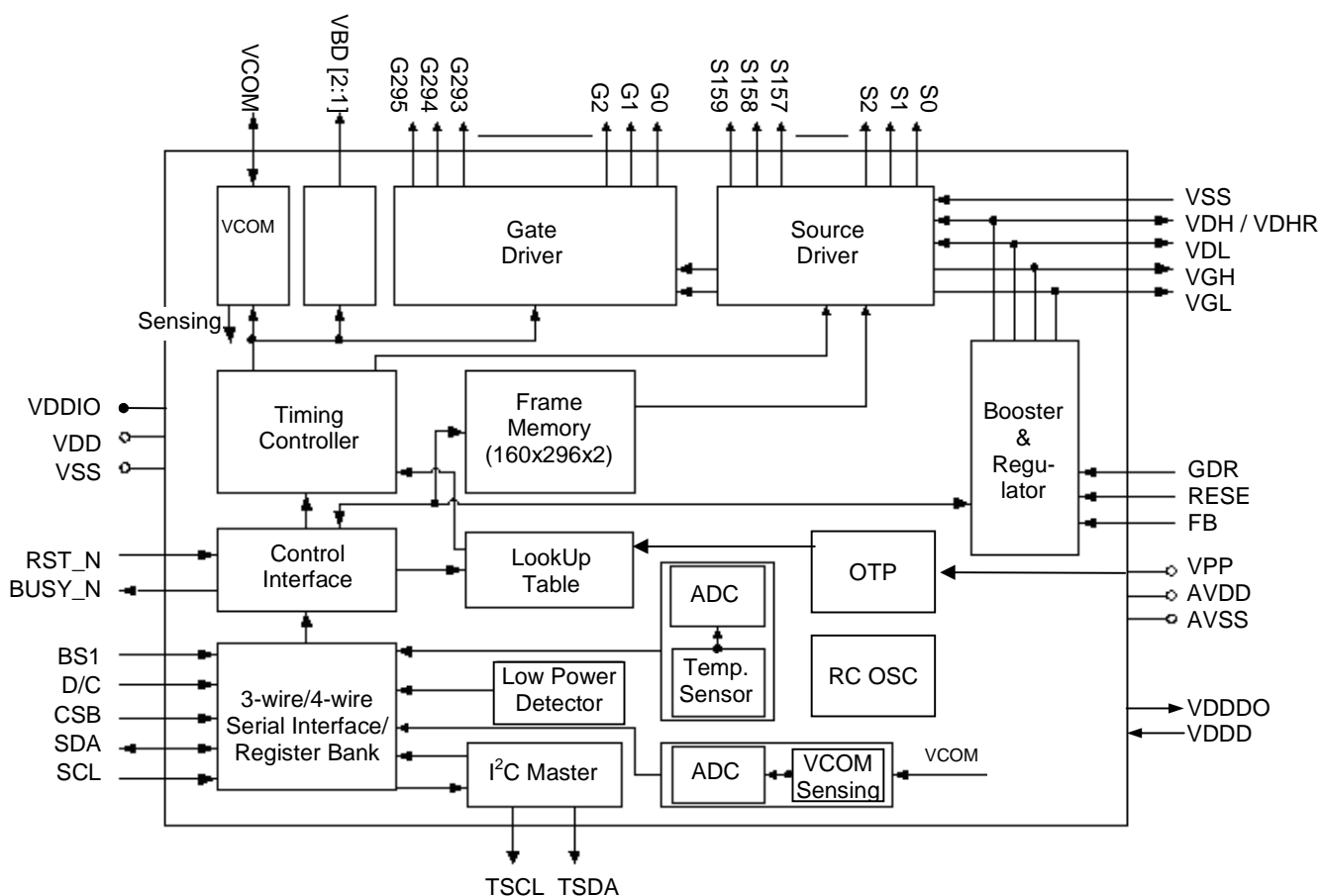
## FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL
- Timing controller supports several all-resolutions
- Resolution:
  - Up to 160 source x 296 gate resolution + 1 border + 1 Vcom
  - 1 bit for white/black and 1 bit for red per pixel
- Cascade: Up to 2 chip cascade mode
- Memory (Max.): 160 x 296 x 2 bits SRAM
- 3-wire/4-wire (SPI) serial interface

- Clock rate up to 20MHz
- Temperature sensor:
  - On-Chip:  $-25 \sim 50^{\circ}\text{C} \pm 2.0^{\circ}\text{C}$  / 8-bit status
  - Off-Chip:  $-55 \sim 125^{\circ}\text{C} \pm 2.0^{\circ}\text{C}$  / 11-bit status ( $I^2C/LM75$ )
- Support LPD, Low Power Detection ( $V_{DD} < 2.5V$ )
- OSC / PLL: On-chip RC oscillator ( $1.625\text{MHz} \pm 5\%$ )
- Vcom:
  - AC-Vcom / DC-Vcom (by LUT)
  - Support Vcom sensing (6-bit digital status)
- Charge Pump: On-chip booster and regulator:
  - VGH: +16V
  - VGL: -16V
  - V<sub>DH</sub>: +2.4 ~ +11.0V (programmable, black/white)
  - V<sub>DL</sub>: -2.4 ~ -11.0V (programmable, black/white)
  - V<sub>DHR</sub>: +2.4 ~ +11.0V (programmable, red)
- Digital supply voltage: 2.3~ 3.6V
- OTP: 4K-byte OTP for LUT
- Package: (TBD)
- COM/SEG bump information
  - Bump pitch: 26  $\mu\text{M}$
  - Bump gap: 14  $\mu\text{M} \pm 3\mu\text{M}$
  - Bump surface: 1200  $\mu\text{M}^2$



### BLOCK DIAGRAM





## PIN DESCRIPTION

Type: I: Input, O: Output, I/O: Input/Output, PWR: Power, C: Capacitor pin

Pin (Pad) Name	Pin Count	Type	Description
<b>POWER SUPPLY PINS</b>			
VDD	7	PWR	Digital power
AVDD (VDDA)	10	PWR	Analog power
VDDIO	10	PWR	IO power
VDDDO	4	PWR	Digital power output (1.8V)
VDDD	4	PWR	Digital power input (1.8V)
VPP	6	PWR	OTP program power (7.75V)
VDM	4	PWR	Analog Ground.
GND	18	PWR	Digital Ground.
GNDA	17	PWR	Analog Ground
<b>LDO PINS</b>			
VDH (VSH)	10	I/O	Positive source driver Voltage (+2.4V ~ +11V)
VDHR	8	I/O	Positive source driver voltage for Red (+2.4V ~ +11V)
VDL (VSL)	10	I/O	Negative source driver voltage (-2.4V ~ -11V)
<b>CONTROL INTERFACE PINS</b>			
BS	1	I	Bus Selection. Select 3-wire / 4-wire SPI interface L: 4-wire interface. <b>H: 3-wire interface. (Default)</b>
RST_N	1	I (Pull-up)	Global reset pin. Low: reset. When RST_N become low, driver will reset. All registers will be reset to their default value, and all driver functions will be disabled. SD output and VCOM will be based on its previous condition; and may have two conditions: 0V or floating.
MS	1	I	Cascade setting pin. L: Slave chip. H: Master chip.
CL	1	I/O	Clock input/output pin. Master: Clock input. Slave: Clock output.
BUSY_N	1	O	Driver busy flag. L: Driver is Busy. H: Host side can send command/data to driver.
<b>MCU INTERFACE (SPI) PINS</b>			
CSB	1	I	Serial communication chip select.
SDA	1	I/O	Serial communication data input/output
SCL	1	I	Serial communication clock input.
DC	1	I	Command/Data input. L: command H: data
<b>I<sup>2</sup>C INTERFACE</b>			
TSCL	2	O (open-drain)	I <sup>2</sup> C clock (External pull-up resistor is necessary.)
TSDA	2	I/O (open-drain)	I <sup>2</sup> C data (External pull-up resistor is necessary.)



Pin (Pad) Name	Pin Count	Type	Description
<b>OUTPUT PINS</b>			
S0~S159 ( S<0>~S<159> )	160	O	Source driver output signals.
G[0..295] ( G<0>~G<295> )	296	O	Gate driver output signals.
VCOM	16	O	VCOM output.
VBD ( VBD<1>~VBD<2> )	2	O	Border output pins.
<b>BOOSTER PINS</b>			
GDR	8	O	N-MOS gate control
RESE	2	P	Current sense input for control loop.
FB	2	P	(Keep Open.)
VGH	12	I/O	Positive Gate voltage.
VGL	16	I/O	Negative Gate voltage.
<b>RESERVED PINS</b>			
TEST1~TEST3	3	I	UltraChip reserved. Leave it floating or connected to VSS.
TESTVDD	1	I	UltraChip reserved. Leave it floating or connected to VSS.
TEST4~TEST7	4	O	UltraChip reserved. Leave it floating.
DUMMY	15	-	UltraChip reserved. Leave it floating.
NC	32	--	Not Connected.



**COMMAND TABLE**

**W/R**: 0: Write Cycle 1: Read Cycle      **C/D**: 0: Command / 1: Data      **D7~D0**: -: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD,SHL,SHD_N,RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1	VDS_EN, VDG_EN VCOM_HV, VGHL_LV[1:0] VDH[5:0] VDL[5:0] VDHR[5:0]	01h
		0	1	--	--	--	--	--	--	#	#		03h
		0	1	--	--	--	--	--	#	#	#		00h
		0	1	--	--	#	#	#	#	#	#		26h
		0	1	--	--	#	#	#	#	#	#		26h
0	1	--	--	#	#	#	#	#	#	03h			
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1	T_VDS_OF	03h
		0	1	--	--	#	#	--	--	--	--		00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure (PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start (BTST)	0	0	0	0	0	0	0	1	1	0	BT_PHA[7:0] BT_PHB[7:0] BT_PHC[5:0]	06h
		0	1	#	#	#	#	#	#	#	#		17h
		0	1	#	#	#	#	#	#	#	#		17h
		0	1	--	--	#	#	#	#	#	#		17h
8	Deep sleep (DSLSP)	0	0	0	0	0	0	0	1	1	1	Check code	07h
		0	1	1	0	1	0	0	1	0	1		A5h
9	Display Start Transmission 1 (DTM1, White/Black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W Pixel Data (160X296): KPXL[1:8] : KPXL[n-1:n]	10h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		:
		0	1	#	#	#	#	#	#	#	#		00h
10	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--		00h
11	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Display Start transmission 2 (DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	Red Pixel Data (160X296): RPXL[1:8] : RPXL[n-1:n]	13h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		:
		0	1	#	#	#	#	#	#	#	#		00h
13	VCOM LUT (LUTC) (45-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	0		20h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	#	#	#	#	#	#	#		ST_XON[6:0]
0	1	--	#	#	#	#	#	#	#	ST_CHV[6:0]	00h		



#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
14	W2W LUT (LUTWW) (42-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	#	#	#	#	#	#	#	#		00h
15	B2W LUT (LUTBW / LUTR) (42-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	0		22h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	#	#	#	#	#	#	#	#		00h
16	W2B LUT (LUTWB / LUTW) (42-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	1		23h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	#	#	#	#	#	#	#	#		00h
17	B2B LUT (LUTBB / LUTB) (42-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	0		24h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	:	:	:	:	:	:	:	:		00h
		0	1	#	#	#	#	#	#	#	#		00h
18	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0	M[2:0], N[2:0]	30h
		0	1	--	--	#	#	#	#	#	#		3Ch
19	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0	LM[10:3] / TSR[7:0] LM[2:0] / -	40h
		1	1	#	#	#	#	#	#	#	#		00h
		1	1	#	#	#	--	--	--	--	--		00h
20	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1	TSE, TO[3:0]	41h
		0	1	#	--	--	--	#	#	#	#		00h
21	Temperature Sensor Write (TSW)	0	0	0	1	0	0	0	0	1	0	WATTR[7:0] WMSB[7:0] WLSB[7:0]	42h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
22	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1	RMSB[7:0] RLSB[7:0]	43h
		1	1	#	#	#	#	#	#	#	#		00h
		1	1	#	#	#	#	#	#	#	#		00h
23	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0	VBD[1:0], DDX[1:0], CDI[3:0]	50h
		0	1	#	#	#	#	#	#	#	#	D7h	
24	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1	LPD	51h
		1	1	--	--	--	--	--	--	--	#		01h
25	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0	S2G[3:0], G2S[3:0]	60h
		0	1	#	#	#	#	#	#	#	#		22h





#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
26	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1	HRES[7:3] VRES[8:0]	61h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	--	--	--	--	--	--	--	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
27	Revision (REV)	0	0	0	1	1	1	0	0	0	0	LUT_REV[7:0]	70h
		0	1	#	#	#	#	#	#	#	#		00h
28	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1	PTL_FLAG, I <sup>2</sup> C_ERR, I <sup>2</sup> C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	71h
		1	1	--	#	#	#	#	#	#	#		02h
29	Auto Measurement Vcom	0	0	1	0	0	0	0	0	0	0	AMVT[1:0], XON, AMVS, AMV, AMVE	80h
		0	1	--	--	#	#	#	#	#	#		10h
30	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1	VV[5:0]	81h
		1	1	--	--	#	#	#	#	#	#		00h
31	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0	VDCS[5:0]	82h
		0	1	--	--	#	#	#	#	#	#		00h
32	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0	HRST[7:3] HRED[7:3] VRST[8:0] VRED[8:0] PT_SCAN	90h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	#	#	#	#	#	0	0	0		00h
		0	1	--	--	--	--	--	--	--	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	--	--	#		00h
		0	1	#	#	#	#	#	#	#	#		00h
33	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
34	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
35	Program Mode (PGM)	0	0	1	0	1	0	0	0	0	0	Check code = A5h	A0h
		0	1	1	0	1	0	0	1	0	1		A5h
36	Active Progrmming (APG)	0	0	1	0	1	0	0	0	0	1		A1h
37	Read OTP (ROTP)	0	0	1	0	1	0	0	0	1	0	Read Dummy Data of Address = 000h : Data of Address = n	A2h
		1	1	--	--	--	--	--	--	--	--		N/A
		1	1	#	#	#	#	#	#	#	#		N/A
		1	1	:	:	:	:	:	:	:	:		N/A
38	Cascade Setting (CCSET)	0	0	1	1	1	0	0	0	0	0	TSFIX, CCEN	E0h
		0	1	--	--	--	--	--	--	#	#		00h
39	Force Temperautre (TSSET)	0	0	1	1	1	0	0	1	0	1	TS_SET[7:0]	E5h
		0	1	#	#	#	#	#	#	#	#		00h

- Note:** (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.
- (2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.
- (3) Commands are processed on the 'stop' condition of the interface.
- (4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.



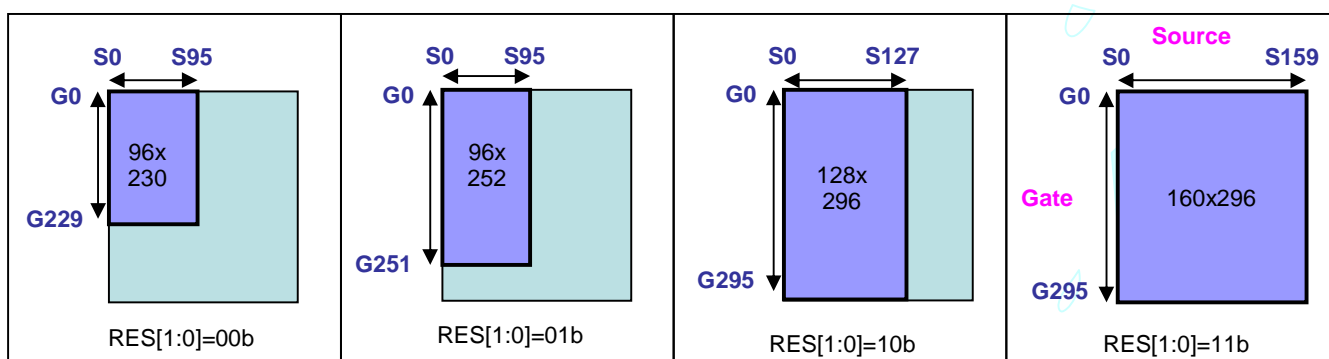
**COMMAND DESCRIPTION**

**[W/R]**: 0: Write Cycle / 1: Read Cycle    **[C/D]**: 0: Command / 1: Data    **[D7-D0]**: -: Don't Care

**(1) PANEL SETTING (PSR) (REGISTER: R00H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG_EN	BWR	UD	SHL	SHD_N	RST_N

**RES[1:0]:** Display Resolution setting (source x gate)  
**00b: 96x230 (Default)** Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.  
**01b: 96x252** Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.  
**10b: 128x296** Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.  
**11b: 160x296** Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.



- (1) Minimum active GD is always G0 regardless of <UD>(R00H).
- (2) Minimum active SD is always S0 regardless of <SHL>(R00H).

**REG\_EN:** LUT selection  
**0: LUT from OTP. (Default)**  
 1: LUT from register.

**BWR:** Black / White / Red  
**0: Pixel with B/W/Red. Run both LU1 and LU2. (Default)**  
 1: Pixel with B/W. Run LU1 only.

**UD:** Gate Scan Direction  
**0: Scan down.** First line to Last line: Gn-1 → Gn-2 → Gn-3 → ... → G0  
**1: Scan up. (Default)** First line to Last line: G0 → G1 → G2 → ... → Gn-1

**SHL:** Source Shift Direction  
**0: Shift left.** First data to Last data: Sn-1 → Sn-2 → Sn-3 → ... → S0  
**1: Shift right. (Default)** First data to Last data: S0 → S1 → S2 → ... → Sn-1

**SHD\_N:** Booster Switch  
**0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.**  
**1: Booster ON (Default)**  
 When SHD\_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD\_N may have two conditions: 0v or floating.

**RST\_N:** Soft Reset  
**1: No effect (Default).** Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V  
 When RST\_N become LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.



**(2) POWER SETTING (PWR) (R01H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1	01h	
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN	03h	
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]		00h	
	0	1	-	-	VDH[5:0]							26h
	0	1	-	-	VDL[5:0]							26h
	0	1	-	VDHR[6:0]								

**VDS\_EN:** Source power selection  
 0 : External source power from VDH/VDL pins  
 1 : Internal DC/DC function for generating VDH/VDL

**VDG\_EN:** Gate power selection  
 0 : External gate power from VGH/VGL pins  
 1 : Internal DC/DC function for generating VGH/VGL

**VCOM\_HV:** VCOM Voltage Level  
 0 : VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC  
 1 : VCOML=VGH, VCOML=VGL

**VGHL\_LV[1:0]:** VGH / VGL Voltage Level selection.

VGHL_LV	VGHL Voltage Level
<b>00 (DEFAULT)</b>	VGH=16V, VGL= -16V
01	VGH=15V, VGL= -15V
10	VGH=14V, VGL= -14V
11	VGH=13V, VGL= -13V

**VDH[5:0]:** Internal VDH power selection for B/W LUT. (Default value: 100110b)

VDH	VDH_V	VDH	VDH_V	VDH	VDH_V	VDH	VDH_V
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	<b>100110</b>	<b>10.0V</b>
000011	3.0 V	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

**VDL[5:0]:** Internal VDL power selection for B/W LUT. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V	VDL	VDL_V	VDL	VDL_V
000000	-2.4 V	001100	-4.8 V	011000	-7.2 V	100100	-9.6 V
000001	-2.6 V	001101	-5.0 V	011001	-7.4 V	100101	-9.8 V
000010	-2.8 V	001110	-5.2 V	011010	-7.6 V	<b>100110</b>	<b>-10.0V</b>
000011	-3.0 V	001111	-5.4 V	011011	-7.8 V	100111	-10.2 V
000100	-3.2 V	010000	-5.6 V	011100	-8.0 V	101000	-10.4 V
000101	-3.4 V	010001	-5.8 V	011101	-8.2V	101001	-10.6 V
000110	-3.6 V	010010	-6.0 V	011110	-8.4 V	101010	-10.8 V
000111	-3.8 V	010011	-6.2 V	011111	-8.6 V	101011	-11.0 V
001000	-4.0 V	010100	-6.4 V	100000	-8.8 V	(others)	-11.0 V
001001	-4.2 V	010101	-6.6 V	100001	-9.0 V		
001010	-4.4 V	010110	-6.8 V	100010	-9.2 V		
001011	-4.6 V	010111	-7.0 V	100011	-9.4 V		



**VDHR[5:0]:** Internal VDL power selection for B/W LUT. (Default value: 000011b)

VDH	VDH_V	VDH	VDH_V	VDH	VDH_V	VDH	VDH_V
000000	2.4 V	001100	4.8 V	011000	7.2 V	100100	9.6 V
000001	2.6 V	001101	5.0 V	011001	7.4 V	100101	9.8 V
000010	2.8 V	001110	5.2 V	011010	7.6 V	100110	10.0V
<b>000011</b>	<b>3.0 V</b>	001111	5.4 V	011011	7.8 V	100111	10.2 V
000100	3.2 V	010000	5.6 V	011100	8.0 V	101000	10.4 V
000101	3.4 V	010001	5.8 V	011101	8.2V	101001	10.6 V
000110	3.6 V	010010	6.0 V	011110	8.4 V	101010	10.8 V
000111	3.8 V	010011	6.2 V	011111	8.6 V	101011	11.0 V
001000	4.0 V	010100	6.4 V	100000	8.8 V	(others)	11.0 V
001001	4.2 V	010101	6.6 V	100001	9.0 V		
001010	4.4 V	010110	6.8 V	100010	9.2 V		
001011	4.6 V	010111	7.0 V	100011	9.4 V		

### (3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF.

SD output and Vcom will remain as previous condition, which may have 2 conditions: 0V or floating.

### (4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]	-	-	-	-	-

**T\_VDS\_OFF[1:0]:** Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default)

01b: 2 frames

10b: 3 frames

11b: 4 frame

### (5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. Refer to the Power ON Sequence section.

### (6) POWER ON MEASURE (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

**(7) BOOSTER SOFT START (BTST) (R06H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	0	0	1	1	0
	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

06h  
17h  
17h  
17h**BTPHA[6:5]:** Soft start period of phase A.

**00b: 10mS**      01b: 20mS      10b: 30mS      11b: 40mS

**BTPHA[4:3]:** Driving strength of phase A

000b: strength 1      001b: strength 2      **010b: strength 3**      011b: strength 4  
000b: strength 5      001b: strength 6      010b: strength 7      011b: strength 8 (strongest)

**BTPHA[2:0]:** Minimum OFF time setting of GDR in phase B

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      **111b: 6.58uS**

**BTPHB[6:5]:** Soft start period of phase B.

**00b: 10mS**      01b: 20mS      10b: 30mS      11b: 40mS

**BTPHB[4:3]:** Driving strength of phase B

000b: strength 1      001b: strength 2      **010b: strength 3**      011b: strength 4  
000b: strength 5      001b: strength 6      010b: strength 7      011b: strength 8 (strongest)

**BTPHB[2:0]:** Minimum OFF time setting of GDR in phase B

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      **111b: 6.58uS**

**BTPHC[4:3]:** Driving strength of phase C

000b: strength 1      001b: strength 2      **010b: strength 3**      011b: strength 4  
000b: strength 5      001b: strength 6      010b: strength 7      011b: strength 8 (strongest)

**BTPHC[2:0]:** Minimum OFF time setting of GDR in phase C

000b: 0.27uS      001b: 0.34uS      010b: 0.40uS      011b: 0.54uS  
100b: 0.80uS      101b: 1.54uS      110b: 3.34uS      **111b: 6.58uS**

**(8) DEEP SLEEP (DSLPL) (R07H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

07h  
A5h

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

**(9) DATA START TRANSMISSION 1 (DTM1) (R10H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes "OLD" data to SRAM.

In B/W/Red mode, this command writes "B/W" data to SRAM.

In Program mode, this command writes "OTP" data to SRAM for programming.

**(10) DATA STOP (DSP) (R11H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data\_flag.

**Data\_flag:** Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (10h) or "Data Stop" (11h) commands and when data\_flag=1, BUSY\_N signal will become "0" and the refreshing of panel starts.

**(11) DISPLAY REFRESH (DRF) (R12H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY\_N signal will become "0" and the refreshing of panel starts.

**(12) DATA START TRANSMISSION 2 (DTM2) (R13H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	:	:	:	:	:	:	:	:
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and write them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes "NEW" data to SRAM.

In B/W/Red mode, this command writes "RED" data to SRAM.

**(13) VCOM LUT (LUTC) (R20H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Build Look-up Table for VCOM (45-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	0	20h	
	0	1	LEVEL SELECT-0		LEVEL SELECT-1		LEVEL SELECT-2		LEVEL SELECT-3		00h	
	0	1	NUMBER OF FRAMES-0									00h
	0	1	NUMBER OF FRAMES-1									00h
	0	1	NUMBER OF FRAMES-2									00h
	0	1	NUMBER OF FRAMES-3									00h
	0	1	TIMES TO REPEAT									00h
	0	1	-	ST_XON[6:0]								00h
	0	1	-	ST_CHV[6:0]								00h

This command stores VCOM Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38:**

Level Selection.

- 00b: VCM\_DC
- 01b: VDH+VCM\_DC (VCOMH)
- 10b: VDL+VCM\_DC (VCOML)
- 11b: Floating

**Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:**

Number of Frames

- 0000 0000b: 0 frame
- : :
- : :
- 1111 1111b: 256 frames

**Bytes 7, 13, 19, 25, 31, 37, 43:**

Times to Repeat

- 0000 0000b: 0 time
- : :
- : :
- 1111 1111b: 256 times

**Bytes 44:**

All Gate ON (ST\_XON [6:0] one hot for each state, ST\_XON [0] for state-1, ST\_XON [1] for state-2 .....)

- 0000 0000b: no All Gate ON
- 0000 0001b: State-1 All Gate ON
- 0000 0011b: State-1 and State2 All Gate ON
- : :

**Bytes 45:**

VCOM High Voltage (ST\_CHV [6:0] one hot for each state, ST\_CHV [0] for state-1, ST\_CHV [1] for state-2 .....)

- 0000 0000b: no VCOM High Voltage
- 0000 0001b: State-1 VCOM High Voltage
- 0000 0011b: State-1 and State2 VCOM High Voltage
- : :

**(14) W2W LUT (LUTWW) (R21H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Build White Look-up Table for W2W (43-byte command, bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1	21h	
	0	1	LEVEL SELECT-0	LEVEL SELECT-1	LEVEL SELECT-2	LEVEL SELECT-3					00h	
	0	1	NUMBER OF FRAMES-0									00h
	0	1	NUMBER OF FRAMES-1									00h
	0	1	NUMBER OF FRAMES-2									00h
	0	1	NUMBER OF FRAMES-3									00h
	0	1	TIMES TO REPEAT									00h

This command stores White-to-White Look-Up Table with 7 groups of data. Each group contains information for one state and is stored with 6 bytes, while the sixth byte indicates how many times that phase will repeat.

**Bytes 2, 8, 14, 20, 26, 32, 38:**

Level Selection.

00b: GND  
01b: VDH  
10b: VDL  
11b: VDHR

**Bytes 3~6, 9~12, 15~18, 21~24, 27~30, 33~36, 39~42:**

Number of Frames

0000 0000b: 0 frame  
:  
:  
1111 1111b: 256 frames

**Bytes 7, 13, 19, 25, 31, 37, 43:**

Times to Repeat

0000 0000b: 0 time  
:  
:  
1111 1111b: 256 times

**(15) B2W LUT (LUTBW / LUTR) (R22H)**

This command builds Look-up Table for Black-to-White. Please refer to W2W LUT (LUTWW) for similar definition details.

**(16) W2B LUT (LUTWB / LUTW) (R23H)**

This command builds Look-up Table for White-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details.

**(17) B2B LUT (LUTBB / LUTB) (R24H)**

This command builds Look-up Table for Black-to-Black. Please refer to W2W LUT (LUTWW) for similar definition details.





**(18) PLL CONTROL (PLL) (R30H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

30h  
3Ch

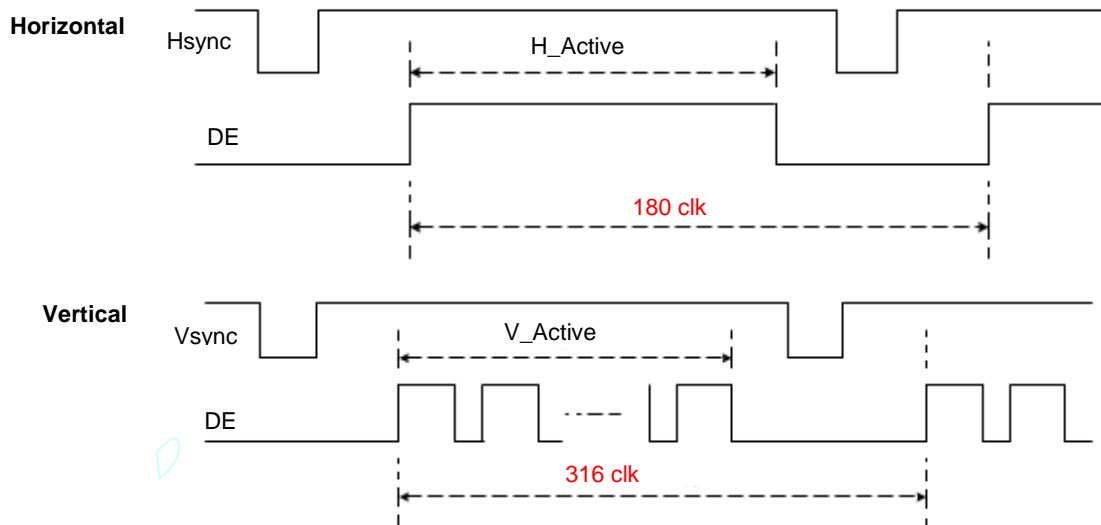
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame rate
1	1	29 Hz
	2	14 Hz
	3	10 Hz
	4	7 Hz
	5	6 Hz
	6	5 Hz
	7	4 Hz
2	1	57 Hz
	2	29 Hz
	3	19 Hz
	4	14 Hz
	5	11 Hz
	6	10 Hz
	7	8 Hz

M	N	Frame rate
3	1	86 Hz
	2	43 Hz
	3	29 Hz
	4	21 Hz
	5	17 Hz
	6	14 Hz
	7	12 Hz
4	1	114 Hz
	2	57 Hz
	3	38 Hz
	4	29 Hz
	5	23 Hz
	6	19 Hz
	7	16 Hz

M	N	Frame rate
5	1	150 Hz
	2	72 Hz
	3	48 Hz
	4	36 Hz
	5	29 Hz
	6	24 Hz
	7	20 Hz
6	1	171 Hz
	2	86 Hz
	3	57 Hz
	4	43 Hz
	5	34 Hz
	6	29 Hz
	7	24 Hz

M	N	Frame rate
7	1	200 Hz
	2	100 Hz
	3	67 Hz
	4	50 Hz (default)
	5	40 Hz
	6	33 Hz
	7	29 Hz



**(19) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0
	1	1	D2	D1	D0	-	-	-	-	-

40h  
00h  
00h

This command reads the temperature sensed by the temperature sensor.

**TS[7:0]:** When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

**D[10:0]:** When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

**(20) TEMPERATURE SENSOR ENABLE (TSE) (R41H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	0	0	1	41h
	0	1	TSE	-	-	-	TO[3:0]				00h	

This command selects Internal or External temperature sensor.

**TSE:** Internal temperature sensor switch

**0: Enable (default)**

**1: Disable; using external sensor.**

**TO[3:0]:** Temperature offset.

**(21) TEMPERATURE SENSOR WRITE (TSW) (R42H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	1	0	42h
	0	1	WATTR[7:0]								00h
	0	1	WMSB[7:0]								00h
	0	1	WLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.

**WATTR: D[7:6]:** I<sup>2</sup>C Write Byte Number  
 00 : 1 byte (head byte only)  
 01 : 2 bytes (head byte + pointer)  
 10 : 3 bytes (head byte + pointer + 1st parameter)  
 11 : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

**D[5:3]:** User-defined address bits (A2, A1, A0)

**D[2:0]:** Pointer setting

**WMSB[7:0]:** MSByte of write-data to external temperature sensor

**WLSB[7:0]:** LSByte of write-data to external temperature sensor

**(22) TEMPERATURE SENSOR READ (TSR) (R43H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Calibrate Temperature Sensor	0	0	0	1	0	0	0	0	1	1	43h
	1	1	RMSB[7:0]								00h
	1	1	RLSB[7:0]								00h

This command reads the temperature sensed by the temperature sensor.

**RMSB[7:0]:** MSByte read data from external temperature sensor

**RLSB[7:0]:** LSByte read data from external temperature sensor



**(23) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)**

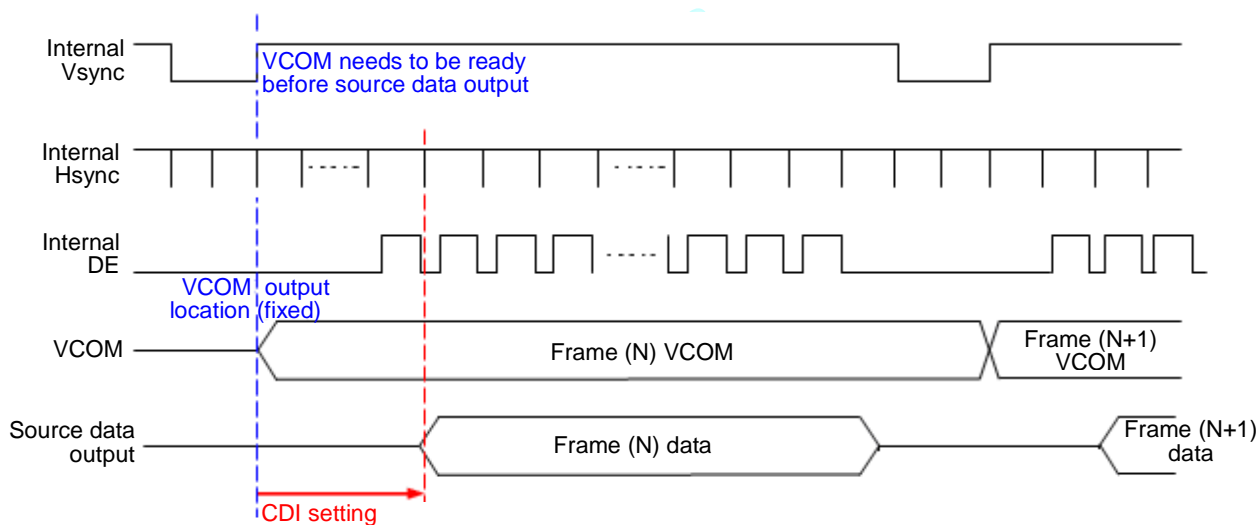
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval between Vcom and Data	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

**VBD[1:0]:** Border data selection  
**DDX[1:0]:** Data polarity.  
 DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.  
 DDX[0] for B/W mode.

**CDI[3:0]:** Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync	1000	9
0001	16	1001	8
0010	15	1010	7
0011	14	1011	6
0100	13	1100	5
0101	12	1101	4
0110	11	1110	3
0111	10 (Default)	1111	2



**(24) LOW POWER DETECTION (LPD) (R51H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

**LPD:** Internal temperature sensor switch  
 0: Low power input (V<sub>DD</sub><2.5V) **1: Normal status (default)**



**(25) TCON SETTING (TCON) (R60H)**

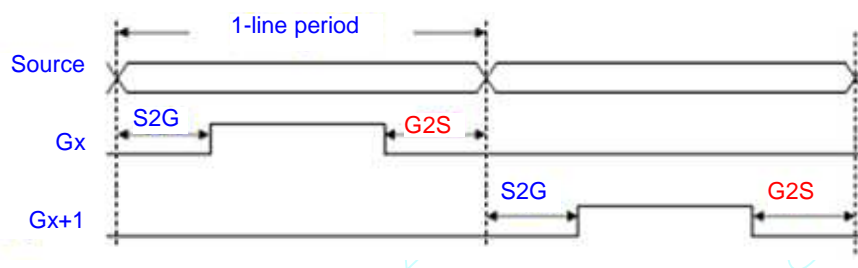
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

**S2G[3:0] or G2S[3:0]:** Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period	S2G[3:0] or G2S[3:0]	Period
0000 b	4	1000 b	36
0001	8	1001	40
0010	12 (Default)	1010	44
0011	16	1011	48
0100	20	1100	52
0101	24	1101	56
0110	28	1110	60
0111	32	1111	64

Period = 660 nS.



**(26) RESOLUTION SETTING (TRES) (R61H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	0	1	1	0	0	0	0	1	
	0	1	HRES[7:3]						0	0	0
	0	1	-	-	-	-	-	-	-	-	VRES[8]

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

**HRES[7:3]:** Horizontal Display Resolution

**VRES[8:0]:** Vertical Display Resolution

Active channel calculation:

GD : First G active = G0; LAST active GD= first active +VRES[8:0] -1

SD : First active channel: =S0 ; LAST active SD= first active +HRES[7:3]\*8-1

EX :128x296

GD: First G active = G0, LAST active GD= 0+296-1= 295; (G295)

SD: First active channel = S0, LAST active SD= 0+128-1=93; (S127)

**(27) REVISION (REV) (R70H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUT_REV							

The LUT\_REV is read from OTP address = 0x001.

**(28) GET STATUS (FLG) (R71H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	PTL_ flag	I <sup>2</sup> C_ERR	I <sup>2</sup> C_ BUSYN	data_ flag	PON	POF	BUSY_N

71h

02h

This command reads the IC status.

**PTL\_FLAG** Partial display status (high: partial mode)

**I<sup>2</sup>C\_ERR:** I<sup>2</sup>C master error status

**I<sup>2</sup>C\_BUSYN:** I<sup>2</sup>C master busy status (low active)

**data\_flag:** Driver has already received all the one frame data

**PON:** Power ON status

**POF:** Power OFF status

**BUSY\_N:** Driver busy status (low active)

**(29) AUTO MEASURE VCOM (AMV) (R80H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]	XON	AMVS	AMV	AMVE	

80h

10h

This command reads the IC status.

**AMVT[1:0]:** Auto Measure Vcom Time

00b: 3s

**01b: 5s (default)**

10b: 8s

11b: 10s

**XON:** All Gate ON of AMV

**0: Gate normally scan during Auto Measure VCOM period. (default)**

1: All Gate ON during Auto Measure VCOM period.

**AMVS:** Source output of AMV

**0: Source output 0V during Auto Measure VCOM period. (default)**

1: Source output VDHR during Auto Measure VCOM period.

**AMV:** Analog signal

**0: Get Vcom value with the VV command (R81h) (default)**

1: Get Vcom value in analog signal.

**AMVE:** Auto Measure Vcom Enable (/Disable)

0: No effect

1: Trigger auto Vcom sensing.

**(30) VCOM VALUE (VV) (R81H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

81h  
00h

This command gets the Vcom value.

**VV[5:0]:** Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

**(31) VCM\_DC SETTING (VDCS) (R82H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set VCM_DC	0	0	1	0	0	0	0	0	1	0
	0	1	-	-	VDCS[5:0]					

82h  
00h

This command sets VCOM\_DC value

**VDCS[5:0]:** VCOM\_DC Setting

VDCS[5:0]	Vcom value
<b>00 0000b</b>	<b>-0.10 V (default)</b>
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

**(32) PARTIAL WINDOW (PTL) (R90H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0		
Set Partial Window	0	0	1	0	0	0	0	0	1	0	90h	
	0	1	HRST[7:3]					0	0	0		00h
	0	1	HRED[7:3]					0	0	0		00h
	0	1	-	-	-	-	-	-	-	VRST[8]		00h
	0	1	VRST[7:0]									00h
	0	1	-	-	-	-	-	-	-	VRED[8]		00h
	0	1	VRED[7:0]									00h
	0	1	-	-	-	-	-	-	-	PT_SCAN		00h

This command sets partial window.

**HRST[7:3]:** Horizontal start bank. (value 00h~13h)

**HRED[7:3]:** Horizontal end bank. (value 00h~13h). HRED must be greater than HRST.

**VRST[8:0]:** Horizontal start bank. (value 000h~127h)

**VRED[8:0]:** Horizontal end bank. (value 000h~127h). VRED must be greater than VRST.

**PT\_SCAN:** 0: Gates scan only inside of the window.

1: Gates scan only outside of the window. (default)

**(33) PARTIAL IN (PTIN) (R91H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial In	0	0	1	0	0	1	0	0	0	1	91h

This command makes the display enter partial mode.

**(34) PARTIAL OUT (PTOUT) (R92H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Partial Out	0	0	1	0	0	1	0	0	1	0	92h

This command makes the display exit partial mode and enter normal mode.

**(35) PROGRAM MODE (PGM) (RA0H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Enter Program Mode	0	0	1	0	1	0	0	0	0	0	A0h
	0	1	1	0	1	0	0	1	0	1	A5h

After this command is issued, the chip would enter the program mode.

The mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

**(36) ACTIVE PROGRAM (APG) (RA1H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Active Program OTP	0	0	1	0	1	0	0	0	0	1	A1h

After this command is transmitted, the programming state machine would be activated.

The BUSY flag would fall to 0 until the programming is completed.

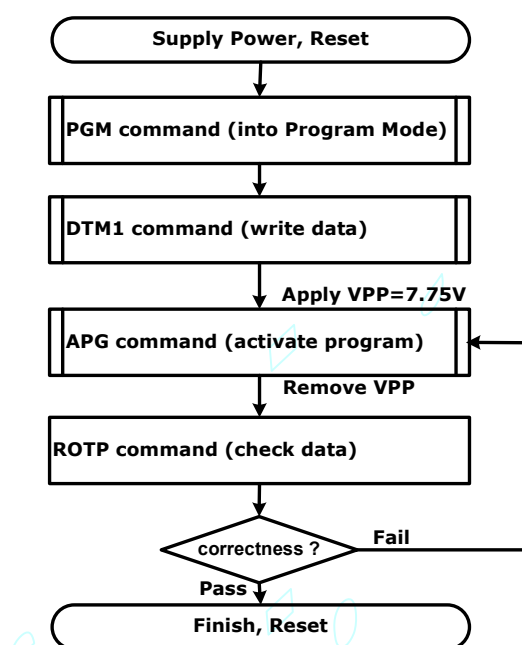


**(37) READ OTP DATA (ROTP) (RA2H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	:							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, the max address = 0xFFF.



The sequence of programming OTP.

**(38) CASCADE SETTING (CCSET) (RE0H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Cascade Option	0	0	1	1	1	0	0	0	0	0
	0	1	-	-	-	-	-	-	TSFIX	CCEN

This command is used for cascade.

**CCEN:** Output clock enable/disable.

**0:** Output 0V at CL pin. (default)

**1:** Output clock at CL pin for slave chip.

**TSFIX:** Let the value of slave's temperature is same as the masters'.

**0:** Temperature value is defined by internal temperature sensor / external LM75. (default)

**1:** Temperature value is defined by TS\_SET[7:0] registers.



**(39) FORCE TEMPERATURE (TSSET) (RE5H)**

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force Temperature Value for Cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

E5h  
00h

This command is used for cascade to fix the temperature value of master and slave chip.



### HOST INTERFACES

#### 3-WIRE SPI

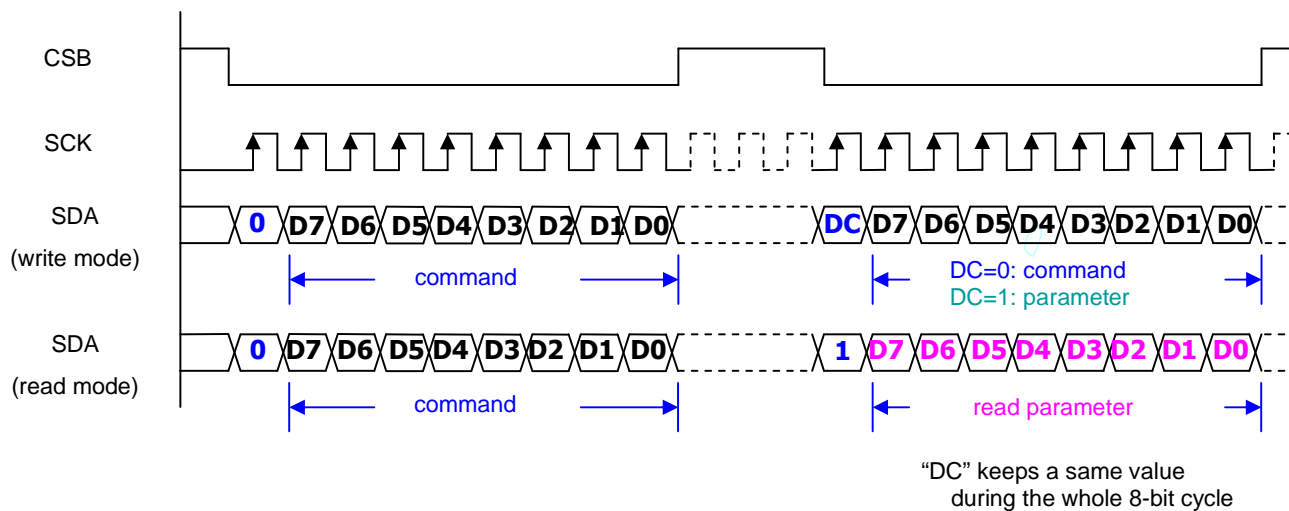


Figure : 3-wire SPI Typical Waveform – BS=1

#### 4-WIRE SPI

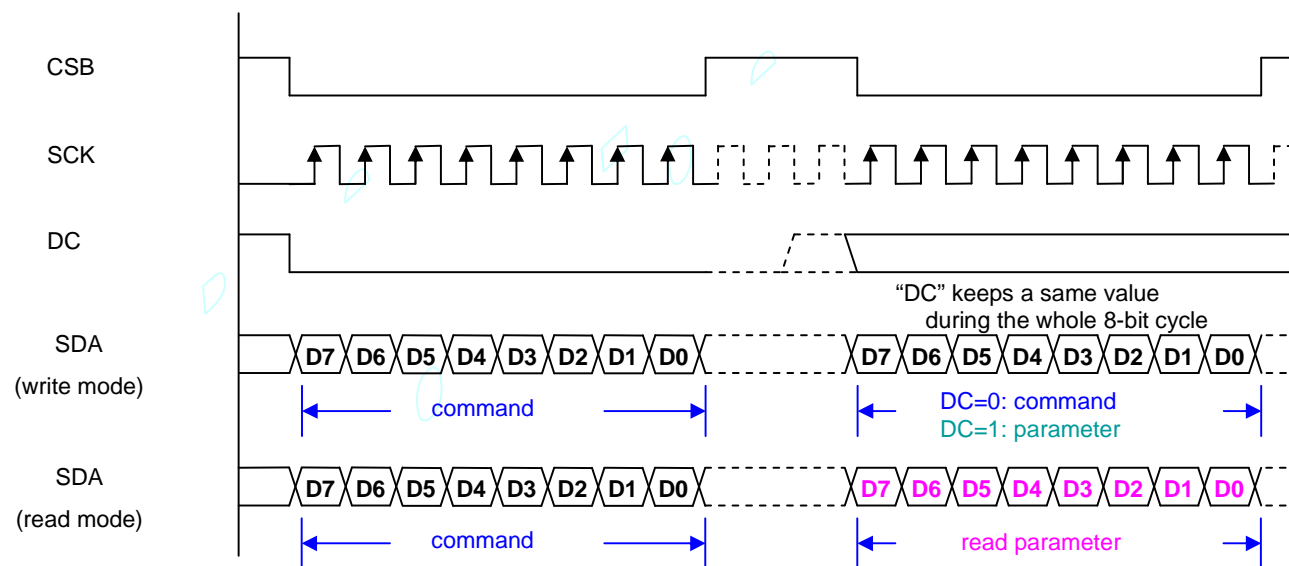
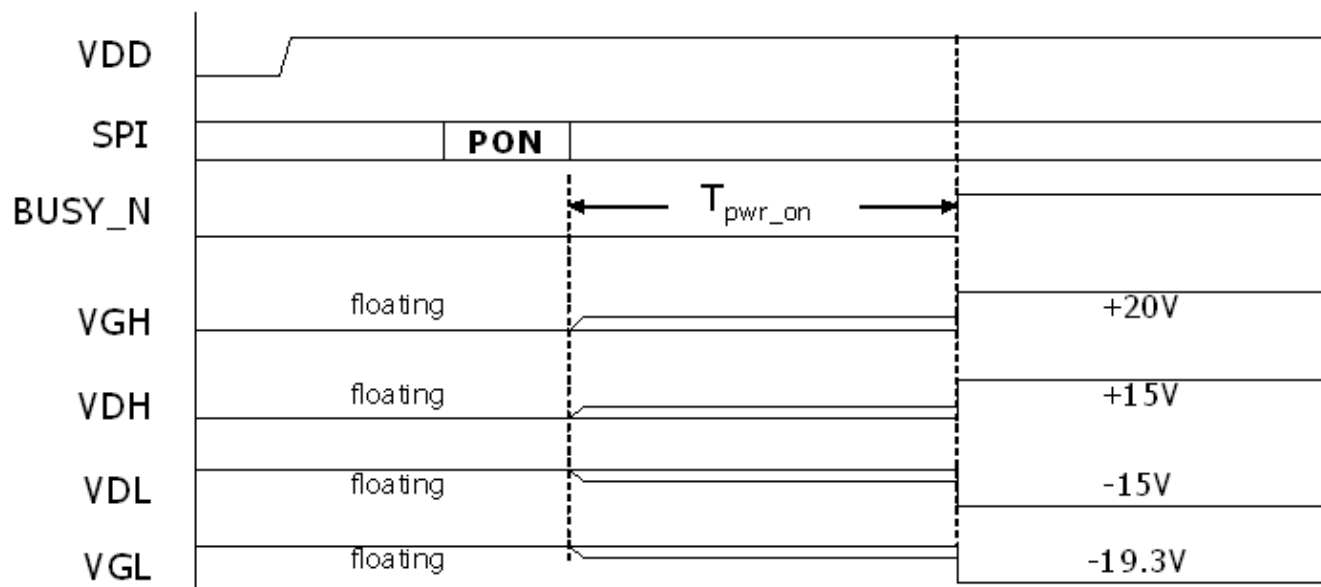


Figure : 4-wire Serial Interface – BS=0



## POWER MANAGEMENT

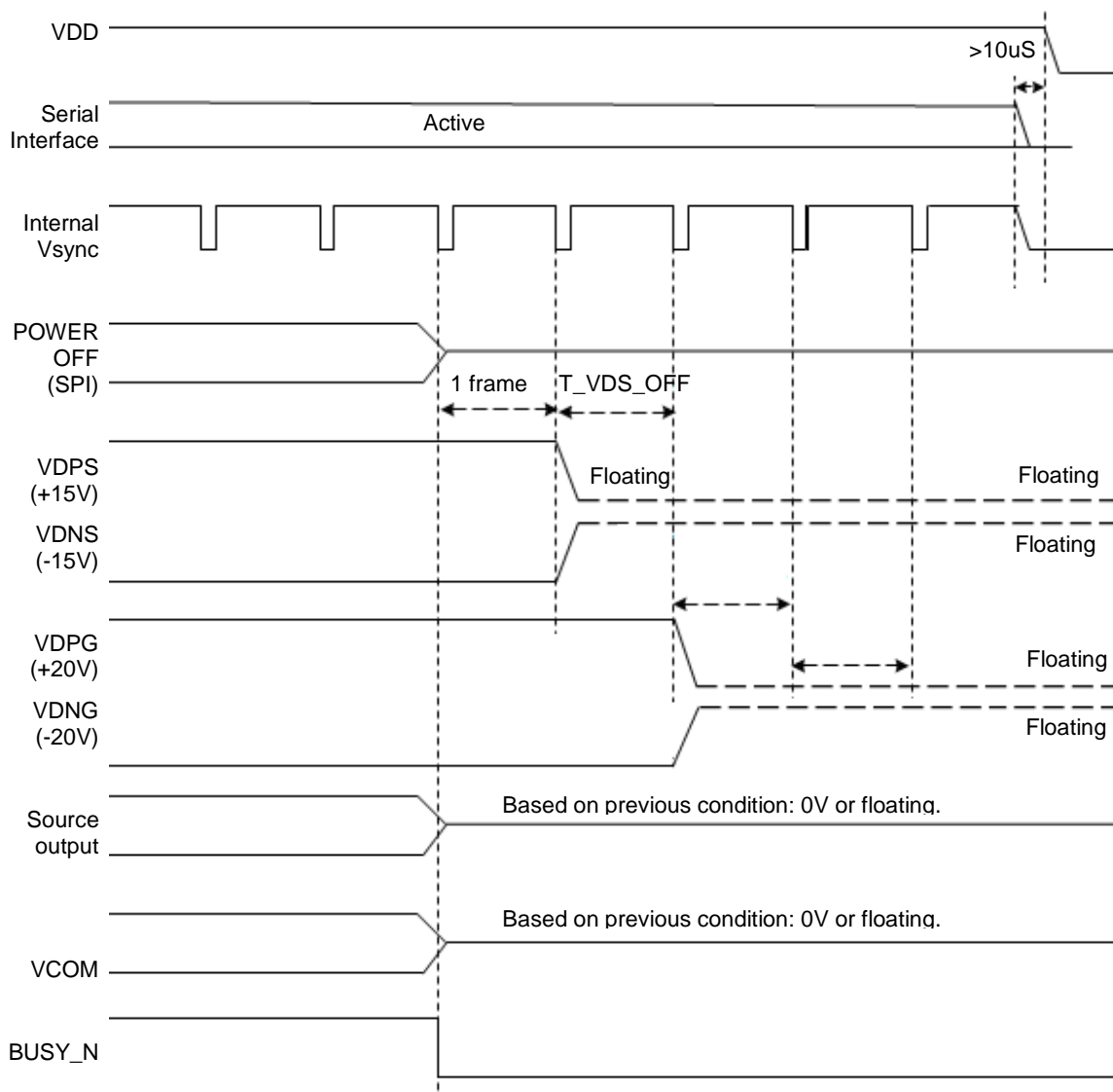
### Power ON Sequence



$T_{pwr\_on} = \sim 80ms$  (default)



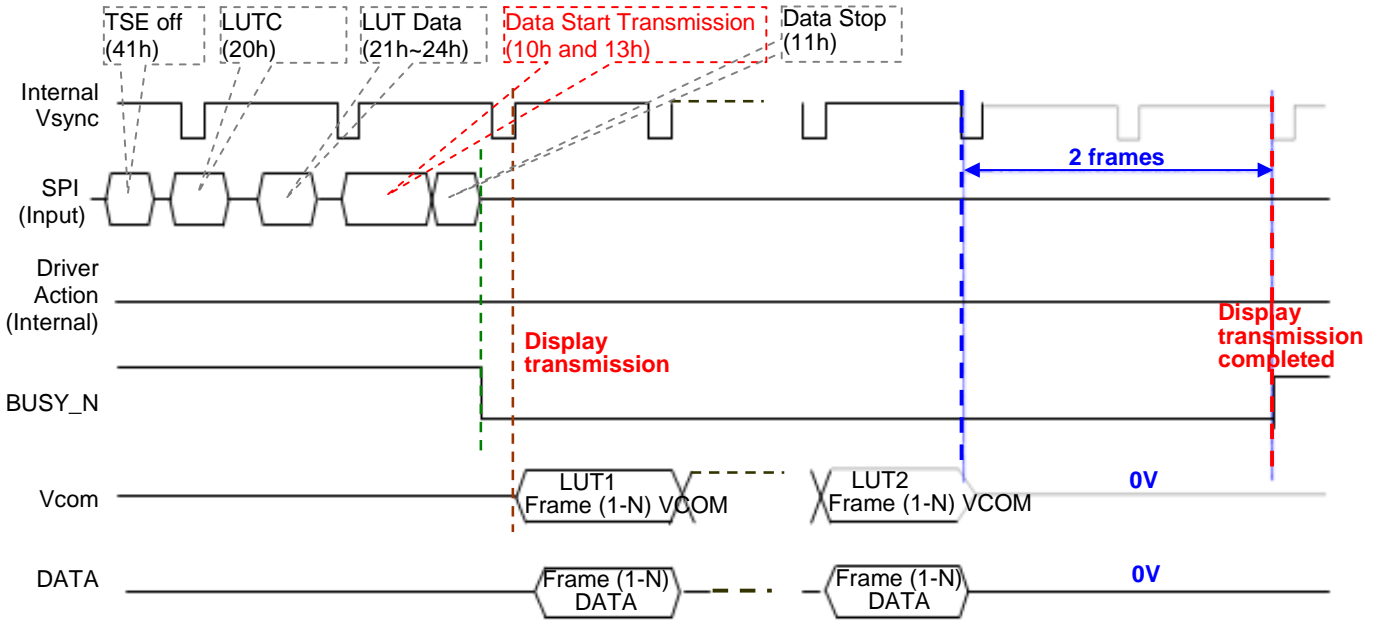
### Power OFF Sequence



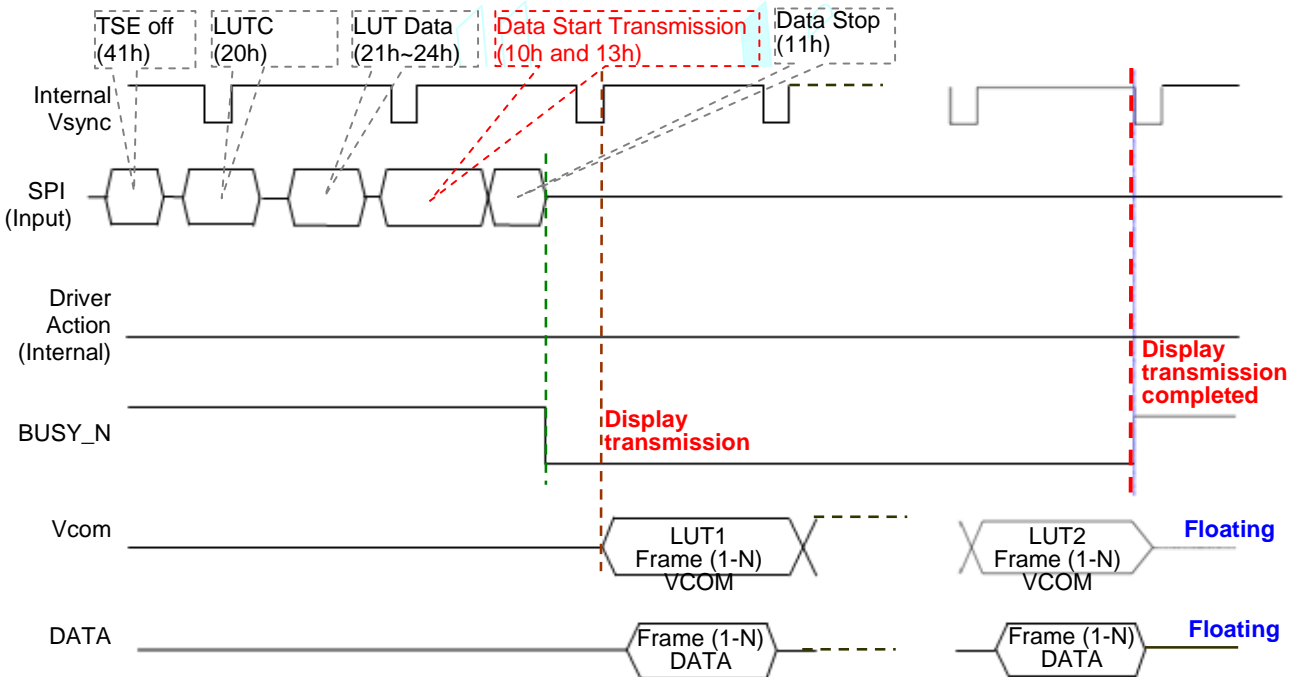


### Data Transmission Waveform

**Example 1:** LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.



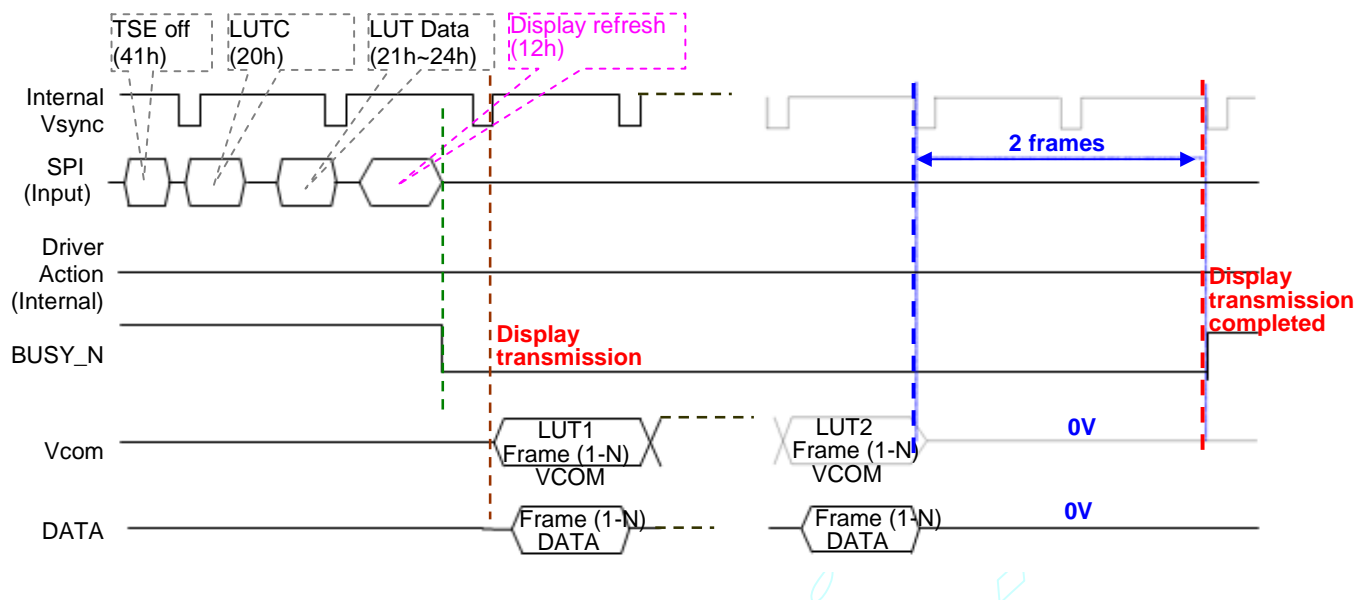
**Example 2:** While level selection in LUT is "11", the driver will float VCOM and data.



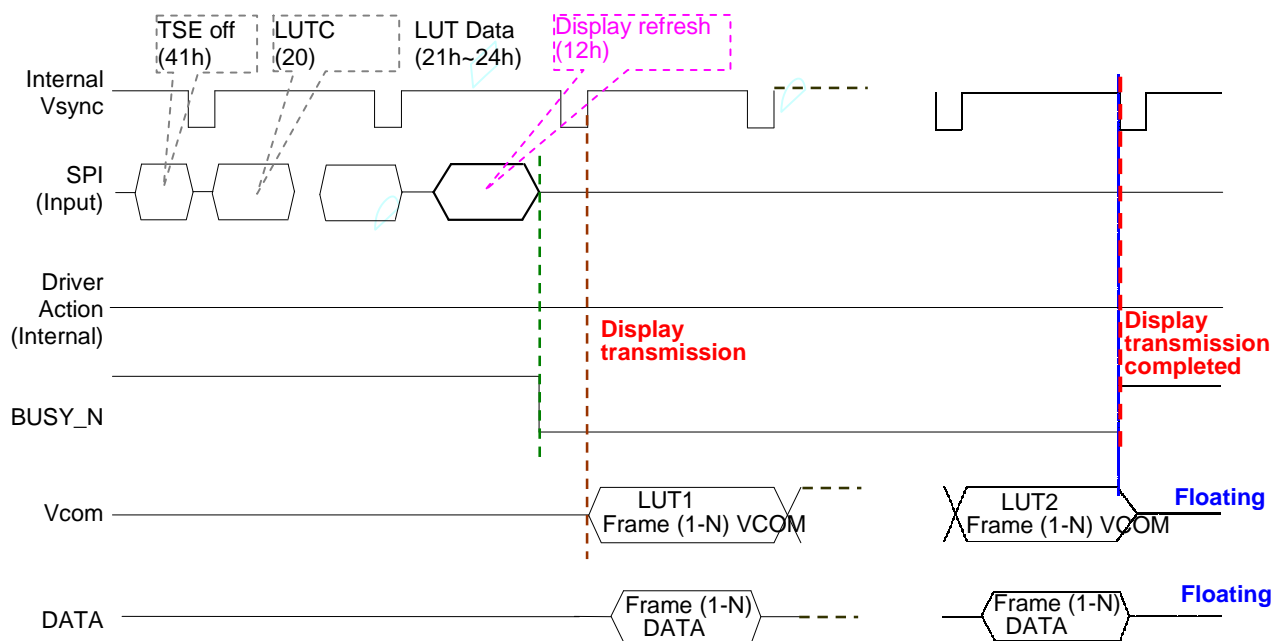


## Display Refresh Waveform

**Example 1:** LUT all states (7 states) complete or phase number=0, the driver will send 2 frame VCOM and data to 0 V.

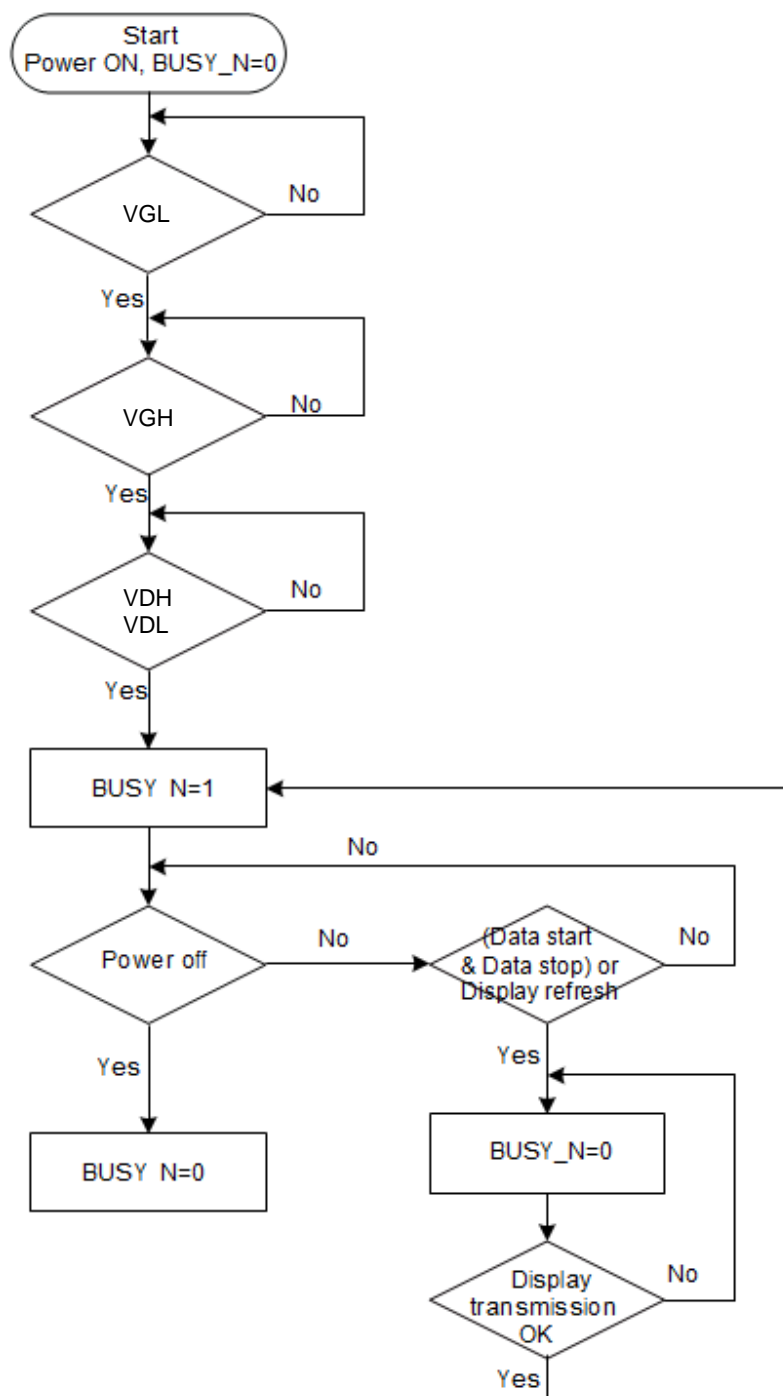


**Example 2:** While level selection in LUT is "11", the driver will float VCOM and data.





**BUSY N Signal Flow Chart**



**BUSY\_N Signal Flow Chart**



## ABSOLUTE MAXIMUM RATINGS

V<sub>DD</sub>/AV<sub>DD</sub> = 2~3.6V (Typ. 3.3V), GND=0V, V<sub>DH</sub>=2.4~11V (Typ. 10V), V<sub>DL</sub>=-2.4~-11V (Typ. -10V), T<sub>A</sub>=0~70°C (Typ. 25°C)

Signal	Item	Min	Max.	Unit
V <sub>DD</sub> , V <sub>IO</sub> , AV <sub>DD</sub> , V <sub>PP</sub>	Logic Supply voltage	-0.3	+6.0	V
V <sub>I</sub>	Digital input range	-0.3	V <sub>DDIO</sub> +40	V
V <sub>GH</sub> -V <sub>GL</sub>	Supply range	V <sub>GL</sub> -0.3	V <sub>GH</sub> +0.3	V
<b>Source</b>				
V <sub>DH</sub>	Analog supply voltage – positive		+20	V
V <sub>DL</sub>	Analog supply voltage -- negative		-20	V
V <sub>DHR</sub>	Analog supply voltage – positive		+20	V
<b>Gate</b>				
V <sub>GH</sub>	Analog supply voltage – positive	-0.3	V <sub>GL</sub> +40	V
V <sub>GL</sub>	Analog supply voltage -- negative	V <sub>GH</sub> -40	0.3	V
I <sub>VGH</sub>	Input rush current for V <sub>DH</sub>	(TBD)	(TBD)	mA
I <sub>VGL</sub>	Input rush current for V <sub>DL</sub>	(TBD)	(TBD)	mA
T <sub>STG</sub>	Storage temperature range	-55	+125	°C

### Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.





## DC CHARACTERISTICS

DIGITAL DC CHARACTERISTICS						
Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
V <sub>IO</sub>	IO supply voltage		2.3	3.3	3.6	V
V <sub>DD</sub>	Supply voltage		2.3	3.3	3.6	V
AV <sub>DD</sub>	DCDC driver supply voltage	DRVU, DRVD	2.3	3.3	3.6	V
V <sub>IL</sub>	LOW Level input voltage	Digital input pins	0	--	0.3xV <sub>DD</sub>	V
V <sub>IH</sub>	HIGH Level input voltage	Digital input pins	0.7xV <sub>IO</sub>	--	V <sub>IO</sub>	V
V <sub>OH</sub>	HIGH Level output voltage	Digital input pins, I <sub>OH</sub> =400uA	V <sub>IO</sub> -0.4	--	--	V
V <sub>OHD</sub>	HIGH Level output voltage	Digital input pins, I <sub>OH</sub> =400uA, DRVD, DRVU	AV <sub>DD</sub> -0.4	--	--	V
V <sub>OL</sub>	LOW Level Output voltage	Digital input pins, I <sub>OL</sub> =-400uA	0	--	0.4	V
I <sub>IN</sub>	Input leakage current	Digital input pins except pull-up, pull-down pin	-1	--	1	uA
R <sub>IN</sub>	Pull-up/down impedance			200		KΩ
I <sub>STVDD</sub>	Digital stand-by current	all stopped (power off mode)	--	0 *	0.1 *	uV
I <sub>VDD</sub>	Digital operating current		--	0.5 *	2.0 *	mV
I <sub>STVIO</sub>	IO stand-by current	all stopped (power off mode)		0.4 *	1.0 *	uV
I <sub>VIO</sub>	IO operating current	No load		-- *	0.2 *	mA
I <sub>STVDD1</sub>	DCDC stand-by current	all stopped (power off mode)		0 *	0.01 *	uA
I <sub>VDD1</sub>	DCDC operating current	fdcdc=250kHz, No load		-- *	0.05 *	mA
		fdcdc=250kHz, External cap: 415pF, NMOS=340pF		0.5 *	1.0 *	
Top	Operating temperature		-30		85	°C

\* TYP. and MAX. values are to be confirmed by design.

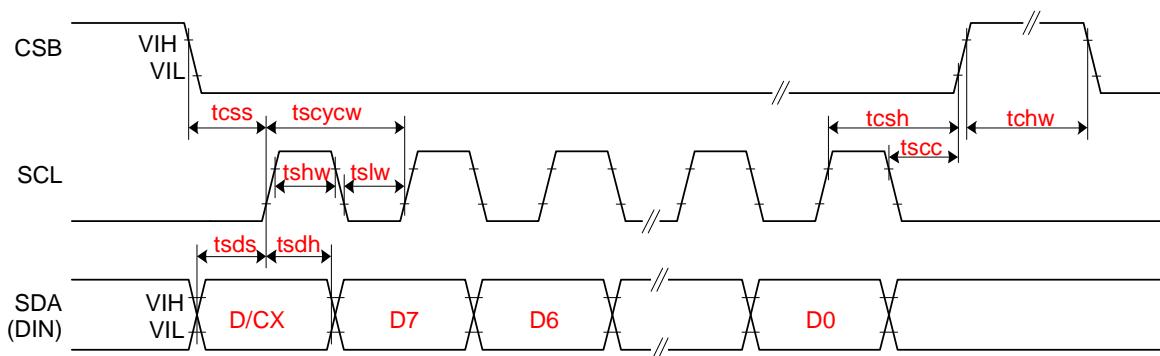


ANALOG DC CHARACTERISTICS						
Symbol	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
VDH	Supply Voltage	For source driver/VCOM		10		V
dVDH	Supply voltage dev		-300	0	+300	mV
VDL	Supply Voltage	For source driver/VCOM		-10		V
dVDL	Supply voltage dev		-300	0	+300	mV
I <sub>dd</sub>	Analog Operating Current	No load,		TBD		mA
V <sub>vd</sub>	Voltage Deviation of Outputs		--	±20	±35	mV
V <sub>dr</sub>	Dynamic Range of Output		0.1	--	VDH-0.1	V
VGH-VGL	Voltage Range of VGH - VGL		12	0	40	V
VGL	VGL voltage Range	For gate driver	-16		-13	V
dVGL	VGL Supply voltage dev		-400	0	+400	mV
VGH	VGH voltage Range	For gate driver	13		VGL+40	V
dVGH	VGH Supply voltage dev		-400	0	+400	mV
I <sub>stVGH</sub>	Positive HV Stand-by Current (power off mode)	Include VDH power With load	-	0 *	0.01 *	μA
I <sub>VGH</sub>	Positive HV Operating Current	Include VDH power With load all SD=L VCOM external resistor divider not included	-	0.7 *	1.1 *	mA
I <sub>VGH</sub>	Positive HV Operating Current	Include VDH power With load all SD=H VCOM external resistor divider not included	-	0.8 *	1.2 *	mA
I <sub>stVGL</sub>	Negative HV Stand-by Current (power off mode)	Include VDPNS power With load	-	0 *	0.01 *	μA
I <sub>VGL</sub>	Negative HV Operating Current	Include VDL power With load all SD=L	-	0.8 *	1.2 *	mA
I <sub>VGL</sub>	Negative HV Operating Current	Include VDL power With load all SD=H	-	0.9 *	1.3 *	mA
I <sub>stVINT1</sub>	VINT1 Stand-by Current (power off mode)		-	0 *	0.01 *	μA
I <sub>VINT1</sub>	VINT1 Operating Current		-	-- *	0.3 *	mA

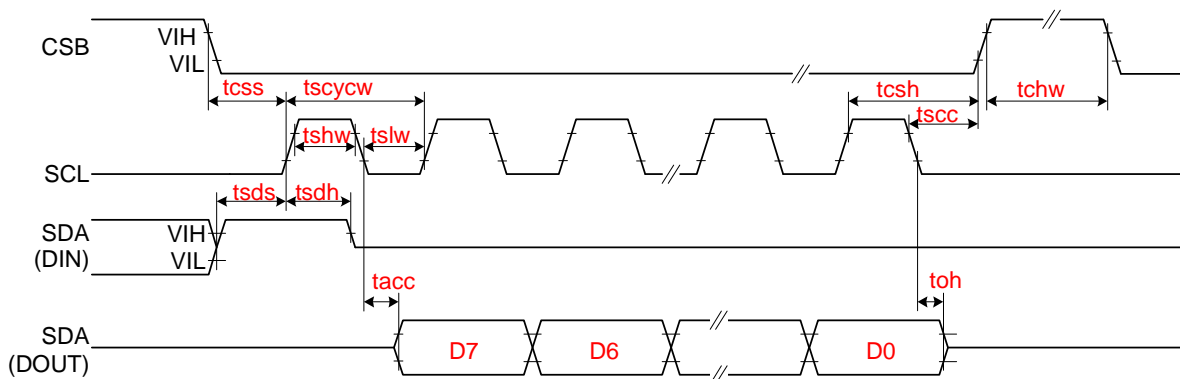
\* TYP. and MAX. values are to be confirmed by design.



### AC CHARACTERISTICS



3-wire Serial Interface – Write

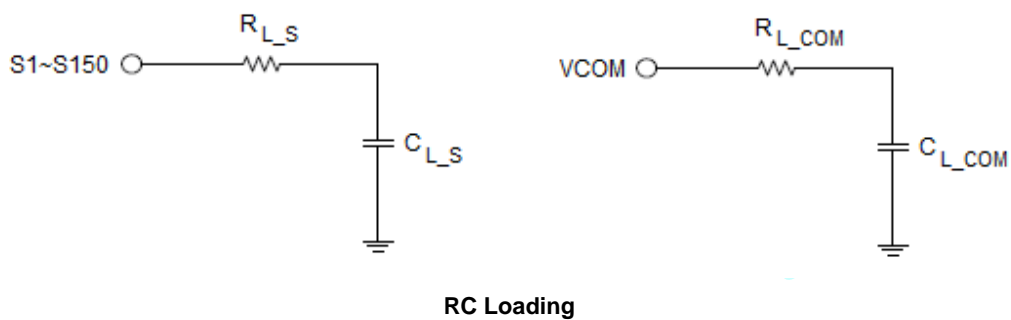


3-wire Serial Interface – Read

SYMBOL	SIGNAL		MIN.	TYP.	MAX.	UNIT
<b>SERIAL COMMUNICATION</b>						
tCSS	CSB	Chip select setup time	60			ns
tCSH		Chip select hold time	65			ns
tSCC		Chip select setup time	20			ns
tCHW		Chip select setup time	40			ns
tSCYCW	SCL	Serial clock cycle (Write)	100			ns
tSHW		SCL "H" pulse width (Write)	35			ns
tSLW		SCL "L" pulse width (Write)	35			ns
tSCYCR		Serial clock cycle (Read)	150			ns
tSHR		SCL "H" pulse width (Read)	60			ns
tSLR		SCL "L" pulse width (Read)	60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time	30			ns
tSDH		Data hold time	30			ns
tACC		Access time	10			ns
tOH		Output disable time	15			ns



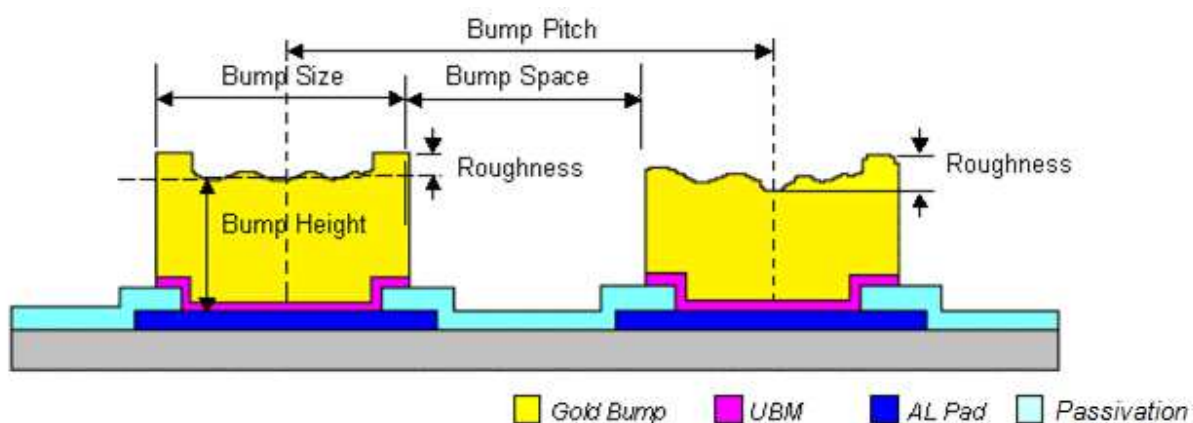
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
<b>DRIVER</b>							
trS		Source driver rise time	99% final value		5		us
tFS		Source driver fall time			5		us
trG		Gate driver rise time	99% final value		5		us
tFG		Gate driver fall time			5		us
trCOM		VCOM rise time	99% final value		1		ms
tFCOM		VCOM fall time			1		ms
<b>RC LOADING</b>							
RL_S		Source driver output loading			TBD		K Ω
CL_S					TBD		pf
RL_G		Gate driver output loading			TBD		KΩ
CL_G					TBD		pf
RL_com		VCOM output loading			TBD		Ω
					TBD		pf



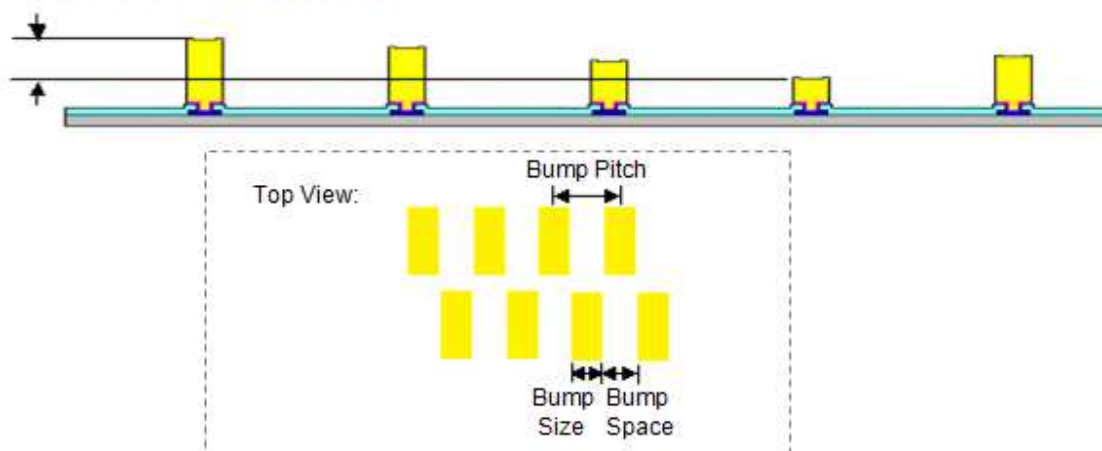


## PHYSICAL DIMENSIONS

Die Size:	$(9531 \mu\text{M} \pm 40\mu\text{M}) \times (981 \mu\text{M} \pm 40\mu\text{M})$
Die Thickness:	$280 \mu\text{M} \pm 20\mu\text{M}$ (Polish)
Die TTV:	$(D_{\text{MAX}} - D_{\text{MIN}})$ within die $\leq 2\mu\text{M}$
Bump Height:	$12 \mu\text{M} \pm 3\mu\text{M}$ $(H_{\text{MAX}} - H_{\text{MIN}})$ within die $\leq 2\mu\text{M}$
Hardness:	$65 \text{ Hv} \pm 15\text{Hv}$
Bump Size:	$12 \mu\text{M} \times 100 \mu\text{M} \pm 2\mu\text{M}$
Bump Area:	$1200 \mu\text{M}^2$
Bump Pitch:	$26 \mu\text{M}$
Bump Gap:	$14 \mu\text{M} \pm 3\mu\text{M}$
Shear:	$\geq 5\text{g/Mil}^2$
Coordinate origin:	Chip center
Pad reference:	Pad center

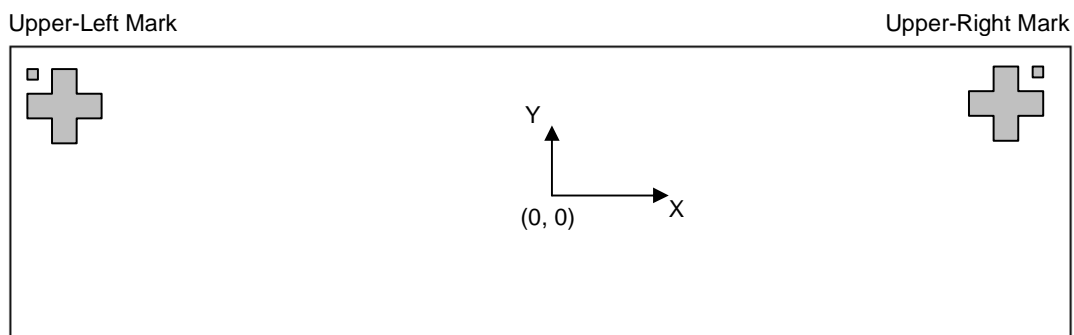


Bump Height Coplanarity within Die

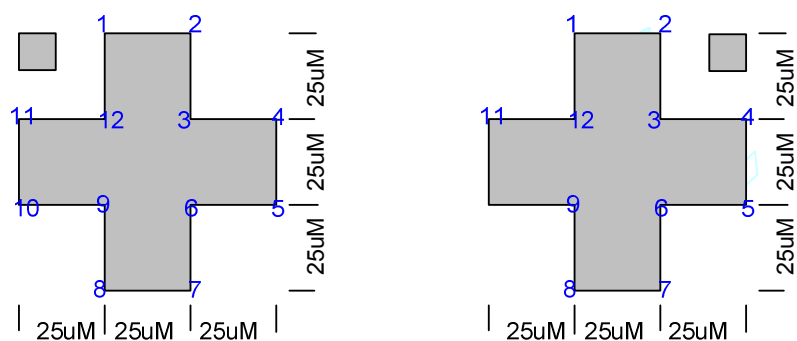


**ALIGNMENT MARK INFORMATION**

Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-4665	390	4665	390
1	-4675	420	4655	420
2	-4655	420	4675	420
3	-4655	400	4675	400
4	-4635	400	4695	400
5	-4635	380	4695	380
6	-4655	380	4675	380
7	-4655	360	4675	360
8	-4675	360	4655	360
9	-4675	380	4655	380
10	-4695	380	4635	380
11	-4695	400	4635	400
12	-4675	400	4655	400



## PAD COORDINATES

No.	Name	X	Y	W	H
1	NC	-4646	-398	28	70
2	VCOM	-4600	-398	28	70
3	VCOM	-4554	-398	28	70
4	VCOM	-4508	-398	28	70
5	VCOM	-4462	-398	28	70
6	VCOM	-4416	-398	28	70
7	VCOM	-4370	-398	28	70
8	VCOM	-4324	-398	28	70
9	VCOM	-4278	-398	28	70
10	VDM	-4232	-398	28	70
11	VGL	-4186	-398	28	70
12	VGL	-4140	-398	28	70
13	VGL	-4094	-398	28	70
14	VGL	-4048	-398	28	70
15	VGL	-4002	-398	28	70
16	VGL	-3956	-398	28	70
17	VGL	-3910	-398	28	70
18	VGL	-3864	-398	28	70
19	VGL	-3818	-398	28	70
20	VGL	-3772	-398	28	70
21	VGL	-3726	-398	28	70
22	VGL	-3680	-398	28	70
23	VGL	-3634	-398	28	70
24	VGL	-3588	-398	28	70
25	VGL	-3542	-398	28	70
26	VGL	-3496	-398	28	70
27	GND	-3450	-398	28	70
28	VSL	-3404	-398	28	70
29	VSL	-3358	-398	28	70
30	VSL	-3312	-398	28	70
31	VSL	-3266	-398	28	70
32	VSL	-3220	-398	28	70
33	VSL	-3174	-398	28	70
34	VSL	-3128	-398	28	70
35	VSL	-3082	-398	28	70
36	VSL	-3036	-398	28	70
37	VSL	-2990	-398	28	70
38	GND	-2944	-398	28	70
39	VGH	-2898	-398	28	70
40	VGH	-2852	-398	28	70
41	VGH	-2806	-398	28	70
42	VGH	-2760	-398	28	70
43	VGH	-2714	-398	28	70
44	VGH	-2668	-398	28	70
45	VGH	-2622	-398	28	70
46	VGH	-2576	-398	28	70
47	VGH	-2530	-398	28	70
48	VGH	-2484	-398	28	70
49	VGH	-2438	-398	28	70
50	VGH	-2392	-398	28	70
51	GND	-2346	-398	28	70
52	VSH	-2300	-398	28	70
53	VSH	-2254	-398	28	70
54	VSH	-2208	-398	28	70
55	VSH	-2162	-398	28	70
56	VSH	-2116	-398	28	70
57	VSH	-2070	-398	28	70
58	VSH	-2024	-398	28	70

No.	Name	X	Y	W	H
59	VSH	-1978	-398	28	70
60	VSH	-1932	-398	28	70
61	VSH	-1886	-398	28	70
62	GND	-1840	-398	28	70
63	VPP	-1794	-398	28	70
64	VPP	-1748	-398	28	70
65	VPP	-1702	-398	28	70
66	VPP	-1656	-398	28	70
67	VPP	-1610	-398	28	70
68	VPP	-1564	-398	28	70
69	VDDD	-1518	-398	28	70
70	VDDD	-1472	-398	28	70
71	VDDD	-1426	-398	28	70
72	VDDD	-1380	-398	28	70
73	VDDDO	-1334	-398	28	70
74	VDDDO	-1288	-398	28	70
75	VDDDO	-1242	-398	28	70
76	VDDDO	-1196	-398	28	70
77	VDM	-1150	-398	28	70
78	VDM	-1104	-398	28	70
79	GND	-1058	-398	28	70
80	GND	-1012	-398	28	70
81	GND	-966	-398	28	70
82	GND	-920	-398	28	70
83	GND	-874	-398	28	70
84	GND	-828	-398	28	70
85	GND	-782	-398	28	70
86	GND	-736	-398	28	70
87	GND	-690	-398	28	70
88	GND	-644	-398	28	70
89	GND	-598	-398	28	70
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93	GND	-414	-398	28	70
94	GND	-368	-398	28	70
95	GND	-322	-398	28	70
96	GND	-276	-398	28	70
97	GND	-230	-398	28	70
98	GND	-184	-398	28	70
99	GND	-138	-398	28	70
100	GND	-92	-398	28	70
101	VDDA	-46	-398	28	70
102	VDDA	0	-398	28	70
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104	VDDA	92	-398	28	70
105	VDDA	138	-398	28	70
106	VDDA	184	-398	28	70
107	VDDA	230	-398	28	70
108	VDDA	276	-398	28	70
109	VDDA	322	-398	28	70
110	VDDA	368	-398	28	70
111	VDD	414	-398	28	70
112	VDD	460	-398	28	70
113	VDD	506	-398	28	70
114	VDD	552	-398	28	70
115	VDD	598	-398	28	70
116	VDD	644	-398	28	70



No.	Name	X	Y	W	H
117	VDD	690	-398	28	70
118	TEST1	736	-398	28	70
119	TEST2	782	-398	28	70
120	VDDIO	828	-398	28	70
121	VDDIO	874	-398	28	70
122	VDDIO	920	-398	28	70
123	VDDIO	966	-398	28	70
124	TEST3	1012	-398	28	70
125	DUMMY	1058	-398	28	70
126	DUMMY	1104	-398	28	70
127	DUMMY	1150	-398	28	70
128	DUMMY	1196	-398	28	70
129	DUMMY	1242	-398	28	70
130	SDA	1288	-398	28	70
131	SCL	1334	-398	28	70
132	GND	1380	-398	28	70
133	CSB	1426	-398	28	70
134	VDDIO	1472	-398	28	70
135	DUMMY	1518	-398	28	70
136	GND	1564	-398	28	70
137	DC	1610	-398	28	70
138	VDDIO	1656	-398	28	70
139	DUMMY	1702	-398	28	70
140	GND	1748	-398	28	70
141	RST_N	1794	-398	28	70
142	BUSY_N	1840	-398	28	70
143	CL	1886	-398	28	70
144	VDDIO	1932	-398	28	70
145	VSYNC	1978	-398	28	70
146	GND	2024	-398	28	70
147	DUMMY	2070	-398	28	70
148	VDDIO	2116	-398	28	70
149	BS	2162	-398	28	70
150	GND	2208	-398	28	70
151	DUMMY	2254	-398	28	70
152	VDDIO	2300	-398	28	70
153	TESTVDD	2346	-398	28	70
154	GND	2392	-398	28	70
155	MS	2438	-398	28	70
156	VDDIO	2484	-398	28	70
157	TSDA	2530	-398	28	70
158	TSDA	2576	-398	28	70
159	TSCL	2622	-398	28	70
160	TSCL	2668	-398	28	70
161	TEST4	2714	-398	28	70
162	TEST5	2760	-398	28	70
163	TEST6	2806	-398	28	70
164	TEST7	2852	-398	28	70
165	VDHR	2898	-398	28	70
166	VDHR	2944	-398	28	70
167	VDHR	2990	-398	28	70
168	VDHR	3036	-398	28	70
169	VDHR	3082	-398	28	70
170	VDHR	3128	-398	28	70
171	VDHR	3174	-398	28	70
172	VDHR	3220	-398	28	70
173	DUMMY	3266	-398	28	70
174	DUMMY	3312	-398	28	70
175	DUMMY	3358	-398	28	70
176	DUMMY	3404	-398	28	70

No.	Name	X	Y	W	H
177	DUMMY	3450	-398	28	70
178	DUMMY	3496	-398	28	70
179	GND	3542	-398	28	70
180	FB	3588	-398	28	70
181	FB	3634	-398	28	70
182	GND	3680	-398	28	70
183	RESE	3726	-398	28	70
184	RESE	3772	-398	28	70
185	GND	3818	-398	28	70
186	GDR	3864	-398	28	70
187	GDR	3910	-398	28	70
188	GDR	3956	-398	28	70
189	GDR	4002	-398	28	70
190	GDR	4048	-398	28	70
191	GDR	4094	-398	28	70
192	GDR	4140	-398	28	70
193	GDR	4186	-398	28	70
194	VDM	4232	-398	28	70
195	VCOM	4278	-398	28	70
196	VCOM	4324	-398	28	70
197	VCOM	4370	-398	28	70
198	VCOM	4416	-398	28	70
199	VCOM	4462	-398	28	70
200	VCOM	4508	-398	28	70
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202	VCOM	4600	-398	28	70
203	NC	4646	-398	28	70
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205	NC	4519	413.5	18	75
206	NC	4498	313.5	18	75
207	NC	4477	413.5	18	75
208	NC	4456	313.5	18	75
209	NC	4435	413.5	18	75
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211	G<2>	4393	413.5	18	75
212	G<4>	4372	313.5	18	75
213	G<6>	4351	413.5	18	75
214	G<8>	4330	313.5	18	75
215	G<10>	4309	413.5	18	75
216	G<12>	4288	313.5	18	75
217	G<14>	4267	413.5	18	75
218	G<16>	4246	313.5	18	75
219	G<18>	4225	413.5	18	75
220	G<20>	4204	313.5	18	75
221	G<22>	4183	413.5	18	75
222	G<24>	4162	313.5	18	75
223	G<26>	4141	413.5	18	75
224	G<28>	4120	313.5	18	75
225	G<30>	4099	413.5	18	75
226	G<32>	4078	313.5	18	75
227	G<34>	4057	413.5	18	75
228	G<36>	4036	313.5	18	75
229	G<38>	4015	413.5	18	75
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231	G<42>	3973	413.5	18	75
232	G<44>	3952	313.5	18	75
233	G<46>	3931	413.5	18	75
234	G<48>	3910	313.5	18	75
235	G<50>	3889	413.5	18	75
236	G<52>	3868	313.5	18	75





No.	Name	X	Y	W	H
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238	G<56>	3826	313.5	18	75
239	G<58>	3805	413.5	18	75
240	G<60>	3784	313.5	18	75
241	G<62>	3763	413.5	18	75
242	G<64>	3742	313.5	18	75
243	G<66>	3721	413.5	18	75
244	G<68>	3700	313.5	18	75
245	G<70>	3679	413.5	18	75
246	G<72>	3658	313.5	18	75
247	G<74>	3637	413.5	18	75
248	G<76>	3616	313.5	18	75
249	G<78>	3595	413.5	18	75
250	G<80>	3574	313.5	18	75
251	G<82>	3553	413.5	18	75
252	G<84>	3532	313.5	18	75
253	G<86>	3511	413.5	18	75
254	G<88>	3490	313.5	18	75
255	G<90>	3469	413.5	18	75
256	G<92>	3448	313.5	18	75
257	G<94>	3427	413.5	18	75
258	G<96>	3406	313.5	18	75
259	G<98>	3385	413.5	18	75
260	G<100>	3364	313.5	18	75
261	G<102>	3343	413.5	18	75
262	G<104>	3322	313.5	18	75
263	G<106>	3301	413.5	18	75
264	G<108>	3280	313.5	18	75
265	G<110>	3259	413.5	18	75
266	G<112>	3238	313.5	18	75
267	G<114>	3217	413.5	18	75
268	G<116>	3196	313.5	18	75
269	G<118>	3175	413.5	18	75
270	G<120>	3154	313.5	18	75
271	G<122>	3133	413.5	18	75
272	G<124>	3112	313.5	18	75
273	G<126>	3091	413.5	18	75
274	G<128>	3070	313.5	18	75
275	G<130>	3049	413.5	18	75
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277	G<134>	3007	413.5	18	75
278	G<136>	2986	313.5	18	75
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287	G<154>	2797	413.5	18	75
288	G<156>	2776	313.5	18	75
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290	G<160>	2734	313.5	18	75
291	G<162>	2713	413.5	18	75
292	G<164>	2692	313.5	18	75
293	G<166>	2671	413.5	18	75
294	G<168>	2650	313.5	18	75
295	G<170>	2629	413.5	18	75
296	G<172>	2608	313.5	18	75

No.	Name	X	Y	W	H
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298	G<176>	2566	313.5	18	75
299	G<178>	2545	413.5	18	75
300	G<180>	2524	313.5	18	75
301	G<182>	2503	413.5	18	75
302	G<184>	2482	313.5	18	75
303	G<186>	2461	413.5	18	75
304	G<188>	2440	313.5	18	75
305	G<190>	2419	413.5	18	75
306	G<192>	2398	313.5	18	75
307	G<194>	2377	413.5	18	75
308	G<196>	2356	313.5	18	75
309	G<198>	2335	413.5	18	75
310	G<200>	2314	313.5	18	75
311	G<202>	2293	413.5	18	75
312	G<204>	2272	313.5	18	75
313	G<206>	2251	413.5	18	75
314	G<208>	2230	313.5	18	75
315	G<210>	2209	413.5	18	75
316	G<212>	2188	313.5	18	75
317	G<214>	2167	413.5	18	75
318	G<216>	2146	313.5	18	75
319	G<218>	2125	413.5	18	75
320	G<220>	2104	313.5	18	75
321	G<222>	2083	413.5	18	75
322	G<224>	2062	313.5	18	75
323	G<226>	2041	413.5	18	75
324	G<228>	2020	313.5	18	75
325	G<230>	1999	413.5	18	75
326	G<232>	1978	313.5	18	75
327	G<234>	1957	413.5	18	75
328	G<236>	1936	313.5	18	75
329	G<238>	1915	413.5	18	75
330	G<240>	1894	313.5	18	75
331	G<242>	1873	413.5	18	75
332	G<244>	1852	313.5	18	75
333	G<246>	1831	413.5	18	75
334	G<248>	1810	313.5	18	75
335	G<250>	1789	413.5	18	75
336	G<252>	1768	313.5	18	75
337	G<254>	1747	413.5	18	75
338	G<256>	1726	313.5	18	75
339	G<258>	1705	413.5	18	75
340	G<260>	1684	313.5	18	75
341	G<262>	1663	413.5	18	75
342	G<264>	1642	313.5	18	75
343	G<266>	1621	413.5	18	75
344	G<268>	1600	313.5	18	75
345	G<270>	1579	413.5	18	75
346	G<272>	1558	313.5	18	75
347	G<274>	1537	413.5	18	75
348	G<276>	1516	313.5	18	75
349	G<278>	1495	413.5	18	75
350	G<280>	1474	313.5	18	75
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356	G<292>	1348	313.5	18	75



No.	Name	X	Y	W	H
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366	NC	1059.5	301	12	100
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369	S<1>	1020.5	420	12	100
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371	S<3>	994.5	420	12	100
372	S<4>	981.5	301	12	100
373	S<5>	968.5	420	12	100
374	S<6>	955.5	301	12	100
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376	S<8>	929.5	301	12	100
377	S<9>	916.5	420	12	100
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387	S<19>	786.5	420	12	100
388	S<20>	773.5	301	12	100
389	S<21>	760.5	420	12	100
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406	S<38>	539.5	301	12	100
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410	S<42>	487.5	301	12	100
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No.	Name	X	Y	W	H
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465	S<97>	-227.5	420	12	100
466	S<98>	-240.5	301	12	100
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468	S<100>	-266.5	301	12	100
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471	S<103>	-305.5	420	12	100
472	S<104>	-318.5	301	12	100
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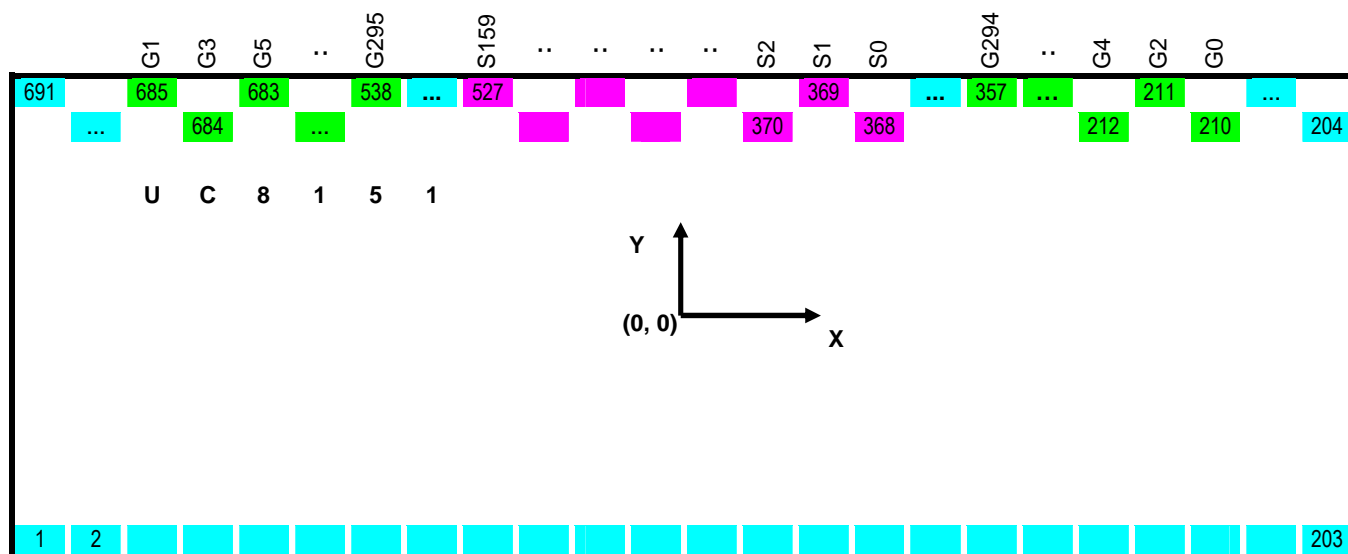
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614	G<143>	-2923	313.5	18	75
615	G<141>	-2944	413.5	18	75
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617	G<137>	-2986	413.5	18	75
618	G<135>	-3007	313.5	18	75
619	G<133>	-3028	413.5	18	75
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622	G<127>	-3091	313.5	18	75
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643	G<85>	-3532	413.5	18	75
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657	G<57>	-3826	413.5	18	75
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661	G<49>	-3910	413.5	18	75
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663	G<45>	-3952	413.5	18	75
664	G<43>	-3973	313.5	18	75
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666	G<39>	-4015	313.5	18	75
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668	G<35>	-4057	313.5	18	75
669	G<33>	-4078	413.5	18	75
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672	G<27>	-4141	313.5	18	75
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674	G<23>	-4183	313.5	18	75
675	G<21>	-4204	413.5	18	75
676	G<19>	-4225	313.5	18	75
677	G<17>	-4246	413.5	18	75
678	G<15>	-4267	313.5	18	75
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682	G<7>	-4351	313.5	18	75
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685	G<1>	-4414	413.5	18	75
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687	NC	-4456	413.5	18	75
688	NC	-4477	313.5	18	75
689	NC	-4498	413.5	18	75
690	NC	-4519	313.5	18	75
691	NC	-4540	413.5	18	75





### TRAY INFORMATION

