Good Display Specifications

Prepared:	AiMing Wei
Checked:	YongCheng Jian
Approved:	Boris Ren
Issue Date:	2016.4.7

Good Display

Dalian Good Display Co., Ltd.

No.17 Gonghua Street, Shahekou District, Dalian 116021 China
Tel: +86-411-84619565 Fax: +86-411-84619585
E-mail: info@good-display.com
Website: www.good-display.com

Table of Content

INTRODUCTION

The IL0371 is an all-in-one gate source driver with an integrated timing controller for ESL application. The source is capable of 3-bit outputs per pixel to support white/black/color. The timing controller provides control signals for the source driver and gate drivers.

The integrated DC-DC converter generates all the necessary source and gate output voltages for VDPS_LV/VDNS_LV (+/-3V~+/- 15V), VDPS/VDNS(+/- 15V) and VDPG/VDNG (+/- 17V ~ +/- 20V). The chip also includes an output buffer for the supply of the common electrode (VCOMAC or VCOMDC). The system is configurable through a 3-wire/4-wire (SPI) serial.

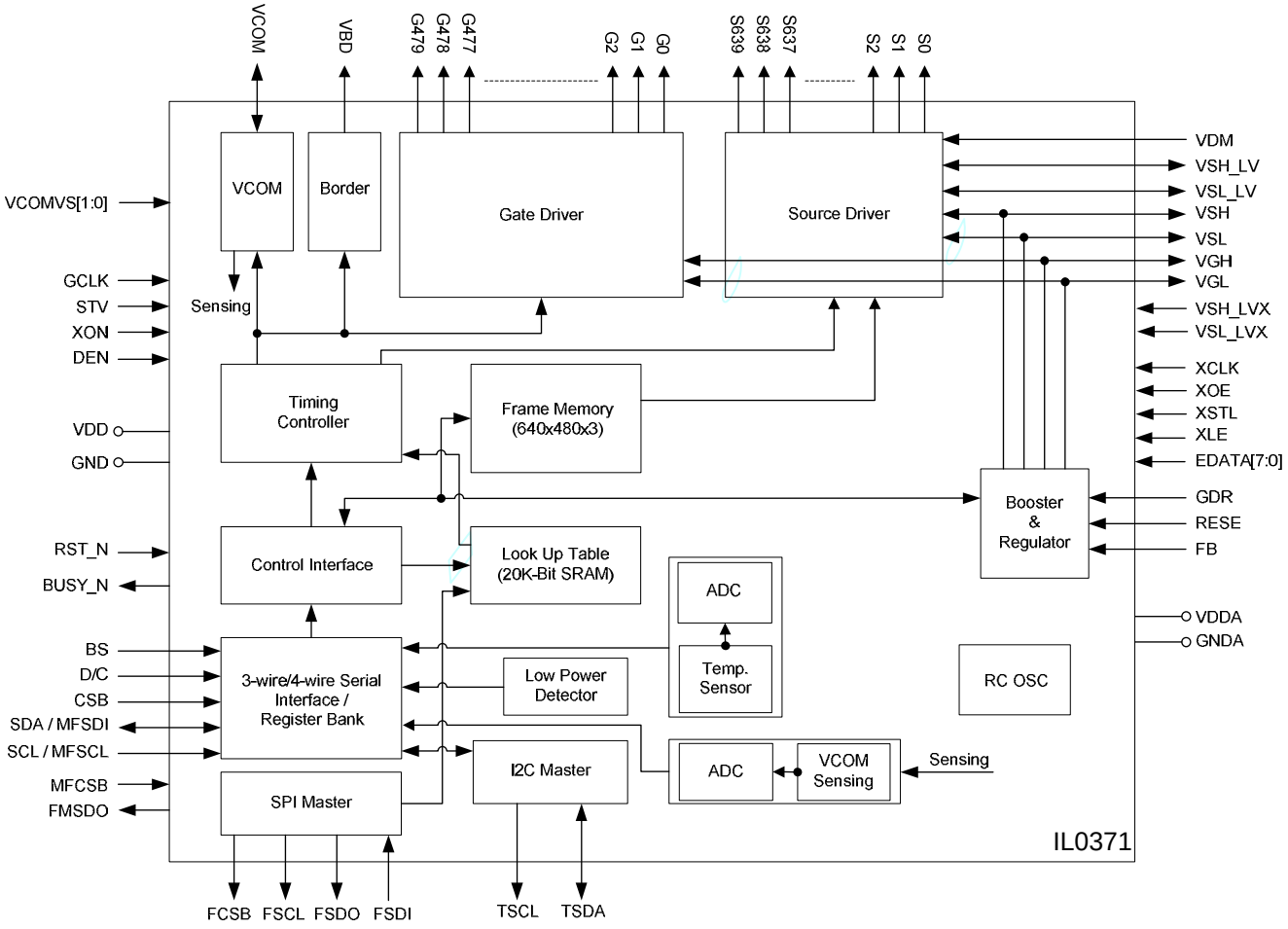
MAIN APPLICATIONS

- E-tag application

FEATURE HIGHLIGHTS

- System-on-chip (SOC) for ESL, including:
- Timing controller support of several resolutions
- Preselect res (640x480, 600x450, 640x448, 600x448)
- Built in Frame memory maximum (640x480x3bit)
- Support LUT
- 640 outputs source driver with 3-bit white/black/red resolution
  - Output dynamic range: VDNS, 0, VDPS, VDNS_LV, VDPS_LV
  - Output deviation: 0.2V
  - 640 channels outputs
  - Left and Right shift capability
- 480 outputs gate driver:
  - 480 channels outputs
  - Up and Down shift capability
  - Output voltage VDNG+40
- 3-wire/4-wire (SPI) serial interface for system configuration
- DC-DC controller for generating the analog power supply
- Common electrode (VCOM AC) level
- External SPI flash/eeprom for WF
- Built-in temperature sensor
- Support I^2C interface for external temperature sensor
- Support low power detection
- Digital supply voltage: 2.3~ 3.6V
- Support frame rate: 200 Hz (max)
- Support pure source & gate driver function
- COG Package

BLOCK DIAGRAM



PIN DESCRIPTION

Type: C: Capacitor pin, I: Input, I/O: Input/Output, M: Mark, O: Output,
PWR: Power, PI: Power Input, PO: Power Output, PS: Power Setting, S: Shorted line

Pin (Pad) Name	Pin Count	Type	Description
SERIAL INTERFACE			
CSB	1	I, Type2	Serial communication chip select.
SDA / MFSDI*	1	I/O, Type5	Serial communication data input. It would bypass to MFSDI by R61H command.
SCL / MFSCL*	1	I, Type2	Serial communication clock input. It would bypass to MFSCL by R61H command.
D/C	1	I, Type2	Serial communication command/parameter input. L: command H: parameter
FMSDO*	1	O, Type1	Serial communication data output. It would bypass to FMSDO by R61H command.
MFCSB*	1	I, Type2	Serial communication chip select. It would bypass to MFCSB by R61H command.
FCSB	1	O, Type1	Serial communication chip select for External Flash/EEPROM.
FSCL	1	O, Type1	Serial communication clock input for External Flash/EEPROM.
FSDI	1	I, Type2	Serial communication clock input for External Flash/EEPROM.
FSDO	1	O, Type1	Serial communication clock output for External Flash/EEPROM.
CONTROL INTERFACE			
BS	1	I, Type2	Input interface setting. Select 3 wire/ 4 wire SPI interface L: 4-wire IF **H: 3-wire IF (Default)**
RST_N	1	I (Pull-up), Type3	Global reset pin. Low reset. When RST_N become low, driver will reset. All register will reset to default value. All driver functions will be disabled. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.
BUSY_N	1	O, Type1	This pin indicates the driver status. L: Driver is busy, data/VCOM is transforming. H: non-busy. Host side can send command/data to driver.
TSCL	2	O	I^2C clock for external temperature sensor.
TSDA	2	I/O	I^2C data for external temperature sensor.

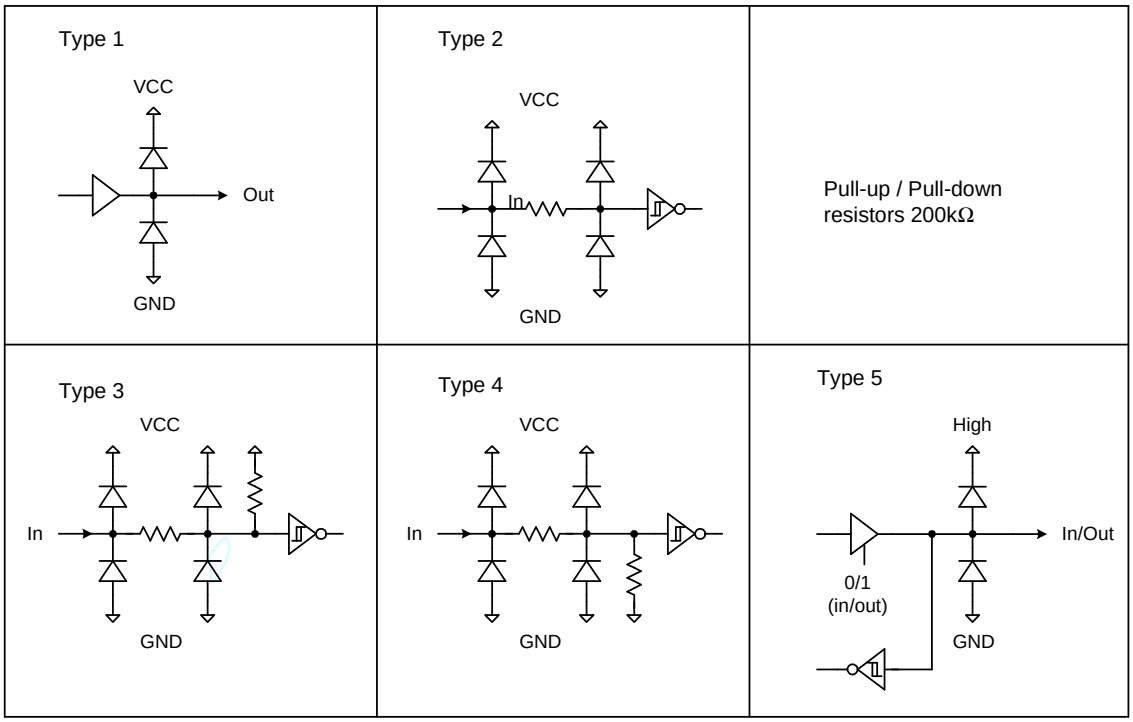
Pin (Pad) Name	Pin Count	Type	Description
SOURCE / GATE DRIVER			
S[0..639]	640	O	Source driver output signals.
G[0..479]	480	O	Gate driver output signals.
VBD	2	O	Border output pin. It will output black WF.
VCOM	16	O	VCOM output. VCOM has four voltage states: 1. (VDPS+VCM_DC) V 2. (VCM_DC) V 3. (VDNS+VCM_DC) V 4. Floating
POWER CIRCUIT			
GDR	6	O	This pin is N-MOS gate control.
RESE	2	PWR	Current sense input for control loop.
FB	2	PWR	Keep open
VGH	20	C	Positive gate voltage
VGL	23	C	Negative gate voltage.
VSH	10	C	Positive source voltage
VSL	10	C	Negative source voltage.
VSH_LV	10	C	Positive source voltage
VSL_LV	10	C	Negative source voltage.
DRIVER INTERFACE			
DEN	1	I	Pure driver mode pin. L: Disable pure driver mode. H: Enable pure driver mode.
XCLK	1	I	Source driver clock input. Data inputs are captured on the rising edge of clock signal.
XOE	1	I	Source driver outputs enabled when OE is logic “H”, Outputs forced to GND when OE is logic “L”. It is asynchronous to clock CLK.
XSTL	1	I	Source driver data shift start pulse
XLE	1	I	Source driver parallel latch enable, transparent when high. It is asynchronous to clock CLK
EDATA[7:0]	8	I	Source driver 8-bit data
GCLK	1	I	Gate driver shift clock pin. The shift register data are shifted synchronously with each rising edge of GCLK.
STV	1	I	Gate driver start pulse
XON	1	I	Driver XON pin

Pin (Pad) Name	Pin Count	Type	Description
POWER SUPPLY			
VDD		PWR	Digital voltage supply
VSS		PWR	Digital ground.
AVDD		PWR	Analog voltage supply
AVSS		PWR	Analog ground.
COMA		S	Internal link together.

Remark:

(1) Pull-up / Pull-down resistors 200KΩ

(2) I/O Pin Structure:



COMMAND TABLE

W/R: 0: Write Cycle 1: Read Cycle C/D: 0: Command / 1: Data D7~D0: –: Don't Care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	--	#	#	#	#	RES[1], RES[0], LUT_EN, UD, SHL, SHD_N, RST_N	07h
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	--	--	--	--	#	#	#	#	EDATA_SEL, EDATA_SET, VGate_EN, VSource_EN	0Fh
		0	1	--	--	--	--	--	#	#	#	VGHL_LV[1:0]	01h
		0	1	--	--	#	#	#	#	#	#	VDPS_LV[5:0]	07h
		0	1	--	--	#	#	#	#	#	#	VDNS_LV[5:0]	07h
3	Power OFF (POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting (PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	--	--	#	#	--	--	--	--	T_VDS_OFF[1:0]	00h
5	Power ON (PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Data Start Transmission 1 (DTM1) (x-byte command)	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	--	#	#	#	--	KPixel1[2:0], KPixel2[2:0]	00h
		0	1	:	:	:	:	:	:	:	:	:	:
		0	1	#	#	#	--	#	#	#	--	Kpixel[2M-1][2:0], Kpixel[2M][2:0]	00h
7	Data Stop (DSP)	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	--	--	--	--	--	--	--	Data_flag	--
8	Display Refresh (DRF)	0	0	0	0	0	1	0	0	1	0		12h
9	PLL control (PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	--	--	#	#	#	#	#	#	M[2:0], N[2:0]	3Ch
10	Temperature Sensor Command (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	D[10:3] / TS[7:0]	00h
		1	1	#	#	#	--	--	--	--	--	D[2:0] / -	00h
11	Temperature Sensor Calibration (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	--	--	#	#	#	#	#	TSE,TO[4:0]	00h
12	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[2:0], DDX, CDI[3:0]	17h
13	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	--	--	--	--	--	--	--	#	LPD	01h
14	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0], G2S[3:0]	22h
15	TCON resolution (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	--	--	--	--	--	#	#	#	HRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	--	--	--	--	--	#	#	#	VRES[9:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
16	SPI flash control (DAM)	0	0	0	1	1	0	0	1	0	1		65h
		0	1	--	--	--	--	--	--	--	#	DAM	00h
17	Revision (REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	--	--	#	#	#	#	#	#	MAN, SHRK, LUT_REV[3:0]	00h
18	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	--	--	#	#	#	#	#	#	I^2C_ERR, I^2C_BUSYN, DATA_FLAG, PON, POF, BUSY_N	--
19	Auto Measurement Vcom (AMV)	0	0	1	0	0	0	0	0	0	0		80h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
		0	1	--	#	#	#	#	#	#	#	VCM_EN, AMVT[1:0], AMVX, AMVS, AMV, AMVE	50h
20	Read Vcom Value(VV)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**		**81h**
		1	1	--	#	#	#	#	#	#	#	VV[6:0]	00h
21	VCM_DC Setting (VDCS)	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**1**	**0**		**82h**
		0	1	--	#	#	#	#	#	#	#	VDCS[6:0]	0Ch

Note: (1) All other register addresses are invalid or reserved by UltraChip, and should NOT be used.

(2) Any bits shown here as 0 must be written with a 0. All unused bits should also be set to zero. Device malfunction may occur if this is not done.

(3) Commands are processed on the 'stop' condition of the interface.

(4) Registers marked 'W/R' can be read, but the contents are written when the SPI command completes – so the contents can be read and altered. The user can subsequently write the register to restore the contents following an SPI read.

(5) All commands are "USABLE" either when BUSY_N=0 or 1, except DSP (R11h) and DRF (R12h), which are only "USABLE" either when BUSY_N=1, ("USELESS" when BUSY_N=0).

* USABLE means that Host can send command/parameter to driver.
* USELESS means that Host cannot send command/parameter to driver.

COMMAND DESCRIPTION

W/R: 0: Write Cycle / 1: Read Cycle C/D: 0: Command / 1: Data D7-D0: –: Don't Care

(1) PANEL SETTING (PSR) (R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting the panel	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	00h
	0	1	RES1	RES0	LUT_EN	-	UD	SHL	SHD_N	RST_N	07h

RES[1:0]: Display Resolution setting (source x gate)
00b: 640x480 (Default)
01b: 600x450
10b: 640x448
11b: 600x448

LUT_EN: LUT selection
0: Using LUT from external Flash.
1: Using LUT from register.

UD: Gate Scan Direction
0: Scan down. First line to Last line: Gn → … … → G1
1: Scan up. (Default) First line to Last line: G1 → … … . → Gn

SHL: Source Shift Direction
0: Shift left. First data to Last data: Sn → … … → S1
1: Shift right. (Default) First data to Last data: S1 → … … . → Sn

SHD_N: Booster Switch
0: DC-DC converter OFF.
1: DC-DC converter ON (Default)
When SHD_N become low, DC-DC will turn OFF. Register and SRAM data will keep until VDD OFF. SD output and VCOM will remain previous condition. It may have two conditions: 0v or floating.

RST_N: Soft Reset
0: The controller is reset. Reset all registers to their default value.
1: Noormal operation (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V
When RST_N become low, driver will reset. All register will reset to default value. Driver all function will disable. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) POWER SETTING (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Selecting Internal/External Power	0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	01h
	0	1	-	-	-	-	EDATA_SEL	EDATA_SET	VGate_EN	VSource_EN	0Fh
	0	1	-	-	-	-	-	-	VGHL_LVL[1:0]		01h
	0	1	-	-	VDPS_LV[5:0]						07h
	0	1	-	-	VDNS_LV[5:0]						07h

EDATA_SEL: EDATA selection for pure driver mode
0 : When EDATA_SET=1, pixel bit =2`b11 output VDPS_L level
1 : When EDATA_SET=1, pixel bit =2`b11 output VDNS_L level (default)

EDATA_SET: EDATA setting for pure driver mode
0 : 3-bit data mode for pure driver
1 : 2-bit data mode for pure driver (default)

VGate_EN: VGate power selection.
0 : External gate power from VDPG and VDNG pin.
1 : Internal DCDC function for generate gate power. (default)

VSource_EN: VSource power selection.
0 : External source power from VDPS and VDNS pin.
1 : Internal DCDC function for generate source power. (default)

VGHL_LVL[1:0]: VGH / VGL Voltage Level selection.

VDPS_LV[5:0]: Internal VDHpower selection for B/W LUT.

VDNS_LV[5:0]: Internal VDL power selection for B/W LUT.

(3) POWER OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning OFF the power	0	0	0	0	0	0	0	0	1	0	02h

After power off command, driver will power off based on the Power OFF Sequence, BUSY_N signal will become “0”.

The Power OFF command will turn off DCDC, T-con, source driver, gate driver, VCOM, temperature sensor, but register and SRAM data will keep until VDD off.

SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(4) POWER OFF SEQUENCE SETTING (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1	03h
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-	00h

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1 frame (Default) 01b: 2 frames 10b: 3 frames 11b: 4 frame

(5) POWER ON (PON) (REGISTER: R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Turning ON the power	0	0	0	0	0	0	0	1	0	0	04h

After the Power ON command, driver will power on based on the Power ON Sequence.

After power on command and all power sequence are ready, then BUSY_N signal will become “1”.

(6) DATA START TRANSMISSION 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Starting data transmission	0	0	0	0	0	1	0	0	0	0	10h
	0	1	KPixel12	KPixel11	KPixel10	Dummy	KPixel22	Kpixel21	Kpixel20	Dummy	00h
	0	1	:	:	:	:	:	:	:	:	00h
	0	1	Kpixel (2M-1)2	Kpixel (2M-1)1	Kpixel (2M-1)0	Dummy	Kpixel (2M)2	Kpixel (2M)1	Kpixel (2M)0	Dummy	00h

This command indicates that user starts to transmit data. Then write to SRAM. While complete data transmission, user must send a DataStop command (R11H). Then the chip will start to send data/VCOM for panel.

Kpixel[1~2M][2:0] :

KPixel[2:0]	Look Up Table
000	LUTB
001	LUTG1
010	LUTG2
011	LUTW
100	LUTR0
101	LUTR1
110	LUTR2
111	LUTR3

(7) DATA STOP (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Stopping data transmission	0	0	0	0	0	1	0	0	0	1	11h
	1	1	data_flag	-	-	-	-	-	-	-	--

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.
1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (10h) or "Data Stop" (11h) commands, BUSY_N signal will become "0".

This command only active when BUSY_N = "1".

(8) DISPLAY REFRESH (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Refreshing the display	0	0	0	0	0	1	0	0	1	0	12h

After this command is issued, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY_N signal will become "0".

This command only active when BUSY_N = "1".

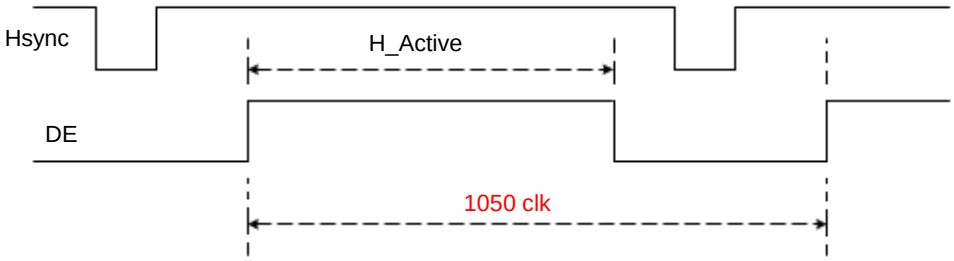
(19) PLL CONTROL (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Controlling PLL	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**	30h
	0	1	-	-	M[2:0]			N[2:0]			3Ch

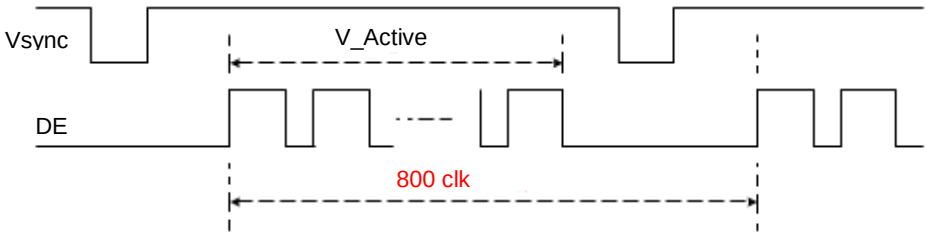
The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

Frame rate (Hz)	
10	Oscclk = 2MHz PLL clock = Oscclk x (M / N)
20	
30	
40	
50 (Default)	
60	
70	
85	
100	
200	

Horizontal



Vertical



(20) TEMPERATURE SENSOR CALIBRATION (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	40h
	1	1	D10	D9/TS6	D8/TS5	D7/TS4	D6 / TS3	D5 / TS2	D4 / TS1	D3 / TS0	00h
	1	1	D2	D1	D0	-	-	-	-	-	00h

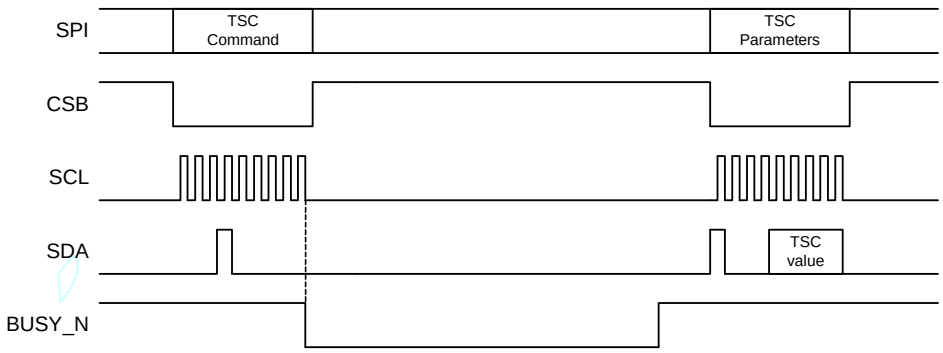
This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

Bit 7~0	Temperature (^{o}C)
0000 0000b	0
0000 0001b	0.5
0000 0010b	1
:	:
0101 1010b	45
:	:
0110 0100b	50
:	:
1100 1110b	-25
:	:
1111 1110b	-1
1111 1111b	-0.5

BUSY_N become low after TSC command. When BUSYN become high, Parameter can be read.



(21) TEMPERATURE SENSOR CALIBRATION (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Calibrate Temperature Sensor	0	0	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**1**	41h
	0	1	TSE	-	-	TO[4:0]					00h

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (default) 1: Disable; using external sensor.

TO[4:0]: Temperature offset.

TO[4]: sign bit 0b: + 1b: -
TO[3:0]: offset value

(22) VCOM AND DATA INTERVAL SETTING (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Interval between Vcom and Data	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	50h
	0	1	VBD[2:0]			DDX	CDI[3:0]				17h

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[2:0]: **V**border control, border output selection

VBD	Border output voltage
000 b	Border floating (Default)
001	Border output LUTB voltage
010	Border output LUTG1 voltage
011	Border output LUTG2 voltage
100	Border output LUTW voltage
101	Border output LUTR1 voltage
110	Border output LUTR2 voltage
111	Border output LUTR3 voltage

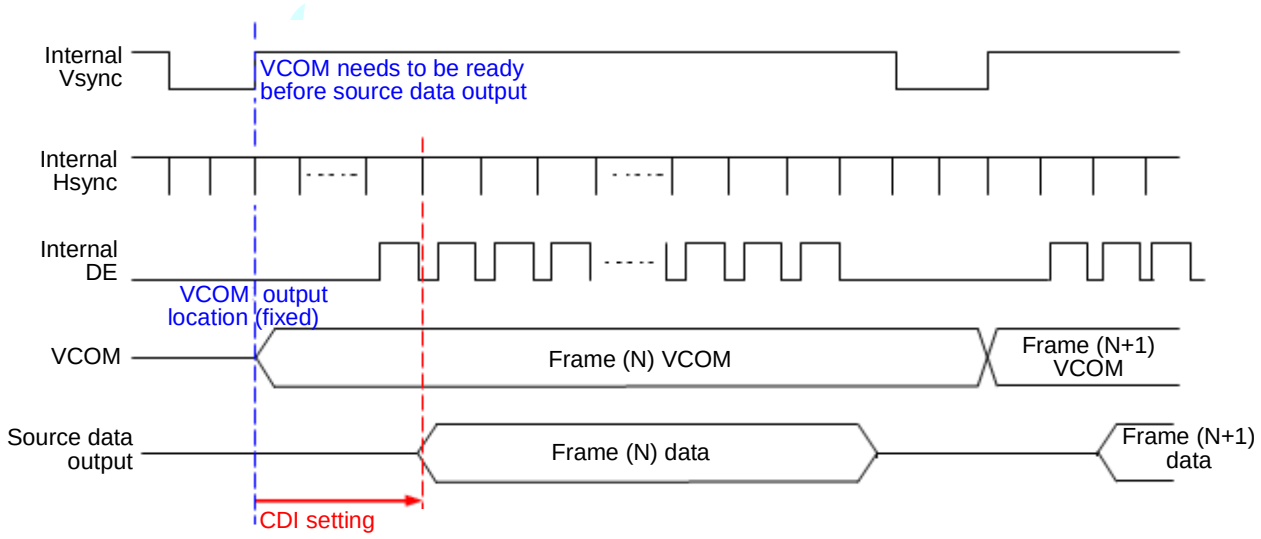
DDX[1:0]: Data polality.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.
DDX[0] for B/W mode.

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync
0001	16
0010	15
0011	14
0100	13
0101	12
0110	11
0111	10 (Default)

CDI[3:0]	Vcom and Data Interval
1000	9
1001	8
1010	7
1011	6
1100	5
1101	4
1110	3
1111	2



(23) LOW POWER DETECTION (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Detect Low Power	0	0	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	51h
	1	1	-	-	-	-	-	-	-	LPD	01h

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Internal temperature sensor switch

0: Low power input (V_{DD}<2.5V) **1: Normal status (default)**

(24) TCON SETTING (TCON) (R60H)

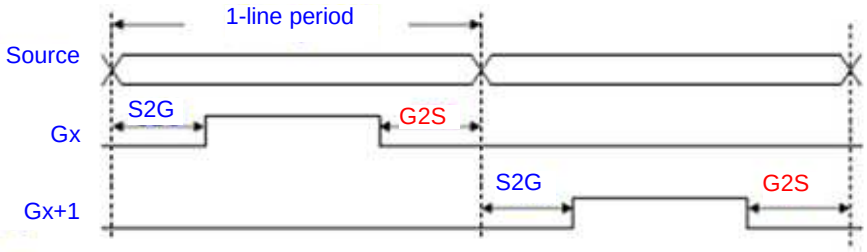
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	60h
	0	1	S2G[3:0]				G2S[3:0]				22h

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period
0000 b	4
0001	8
0010	**12 (Default)**
0011	16
0100	20
0101	24
0110	28
0111	32
1000	36
1001	40
1010	44
1011	48
1100	52
1101	56
1110	60
1111	64

Period = 660 nS.



(25) RESOLUTION SETTING (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set Display Resolution	0	0	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**1**	61h
	0	1	HRES[7:0]								00h
	0	1	-	-	-	-	-	-	HRES[9:8]		00h
	0	1	VRES[7:0]								00h
	0	1	-	-	-	-	-	-	-	VRES[8]	00h

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[9:0]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

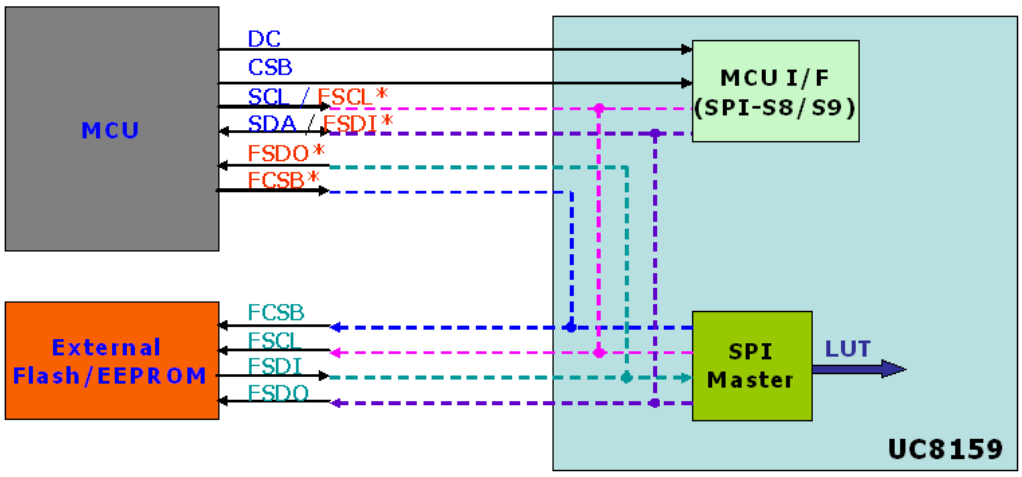
Resolution setting (R61H) has higher priority than RES[1:0] (R00H). Resolution should be even number.

(26) SPI FLASH CONTROL (DAM) (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Sensing Temperature	0	0	**0**	**1**	**1**	**0**	**0**	**1**	**0**	**1**	65h
	0	1	-	-	-	-	-	-	-	DAM	22h

This command defines MCU host direct access external memory mode.

DAM: 0: Disable (Default)
1: Enable. By pass FSCL*, FSDI*, FSDO*, AND FCSB* to external flash.



(27) REVISION (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Chip Revision	0	0	0	1	1	1	0	0	0	0	70h
	1	1	-	-	MAN	SHRK	REV[3:0]				00h

The REV is read from OTP address = 0x001.

MAN:

SHRK: Shrink revision or not. **0: Non-shrink revision (default)** 1: Shrink revision

REV[3:0]: Chip Revision.

(28) GET STATUS (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Read Flags	0	0	0	1	1	1	0	0	0	1	71h
	1	1	-	-	I2C_ ERR	I2C_ BUSYN	Data_ flag	PON	POF	BUSY_N	

This command reads the IC status.

I2C_ERR: I^2C master error status

I2C_BUSYN: I^2C master busy status (low active)

Data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(29) AUTO MEASURE VCOM (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0	80h
	0	1	-	VCM_EN	AMVT[1:0]		AMVX	AMVS	AMV	AMVE	50h

This command reads the IC status.

VCM_EN: VCOM output Enable

0: VCOM floating. **1: VCOM output.** (default)

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s **01b: 5s (default)**
10b: 8s 11b: 10s

AMVX: Auto Measure VCOM without XON function

0: Measure VCOM without XON function. (Gate scanning) (default)
1: Measure VCOM without XON function. (All Gate ON)

AMVS: Source output of AMV

0: Set Source output to 0V during Auto Measure VCOM period. (default)
1: Set Source output to 3V (or VDPS_L) during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)
1: Get Vcom value in analog signal.

AMVE: Auto Measure Vcom Enable (/Disable)

0: Disabled 1: Enabled

(30) VCOM VALUE (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1	81h
	1	1	-	VV[6:0]							00h

This command gets the Vcom value.

VV[6:0]: Vcom Value Output

VV[6:0]	Vcom value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.10 V
000 0011b	-0.15 V
000 0100b	-0.20 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

(31) VCM_DC SETTING (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	
Set VCM_DC	0	0	1	0	0	0	0	0	1	0	82h
	0	1	-	VDCS[6:0]							0Ch

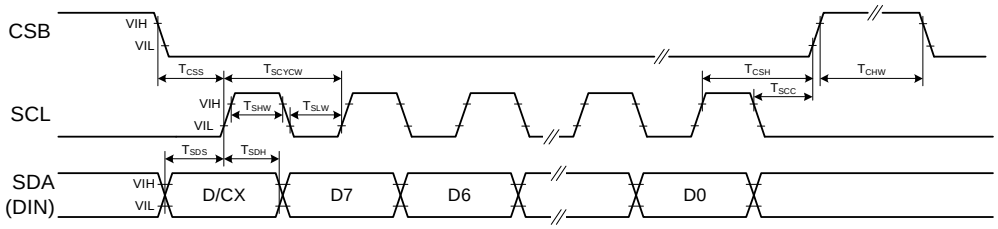
This command sets VCOM_DC value.

VDCS[6:0]: VCOM_DC Setting

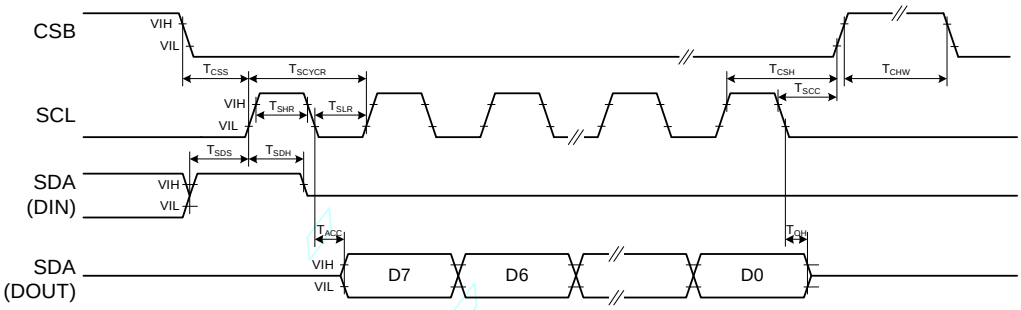
VDCS[6:0]	Vcom_DC value
000 0000b	(Reserved)
000 0001b	(Reserved)
000 0010b	-0.2 V
000 0011b	-0.3 V
000 0100b	-0.4 V
:	:
101 0000b	-4.0 V
(others)	-4.0 V

HOST INTERFACES

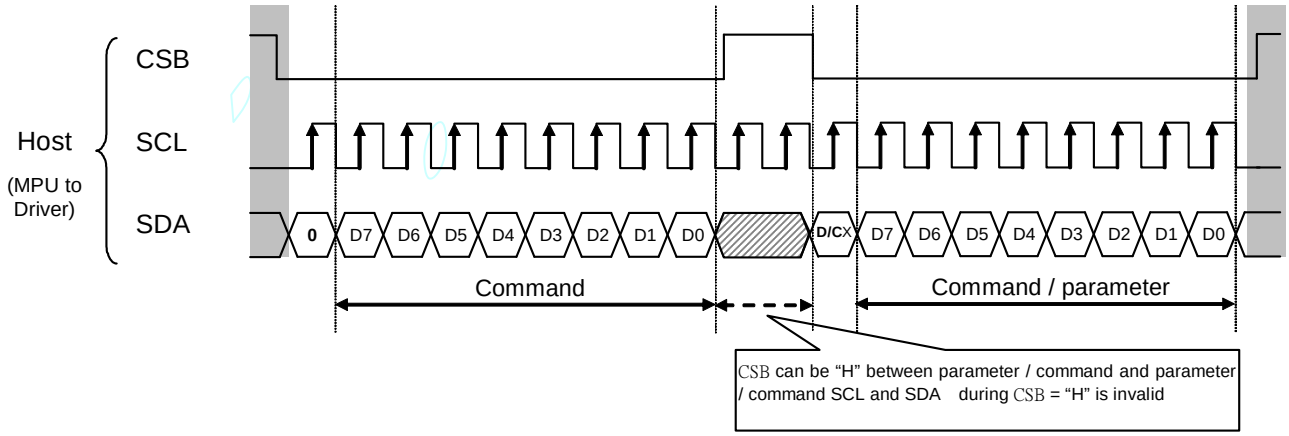
3-WIRE SPI



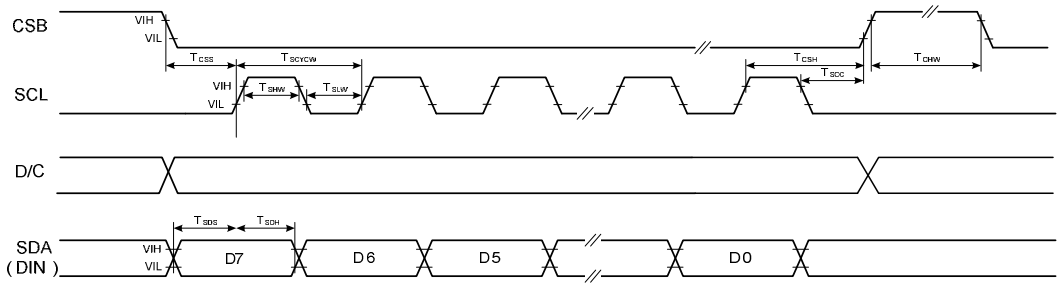
3 pin serial interface characteristics (write mode)



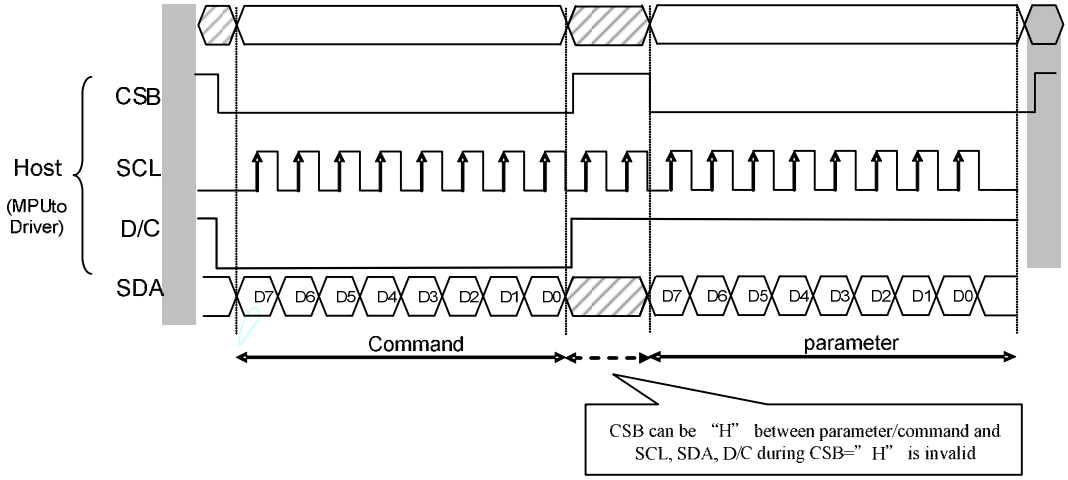
3 pin serial interface characteristics (read mode)



4-WIRE SPI

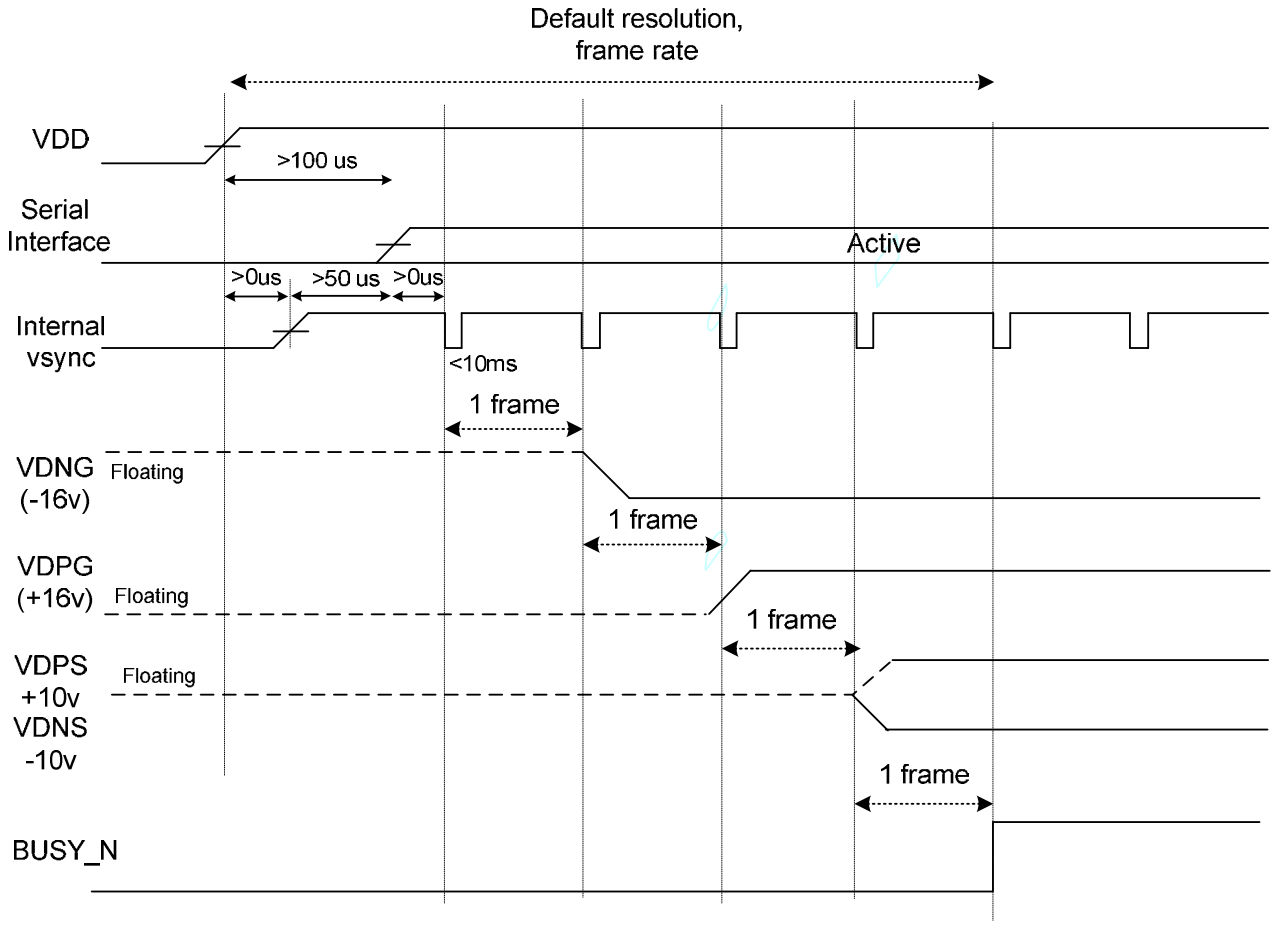


4 pin serial interface characteristics

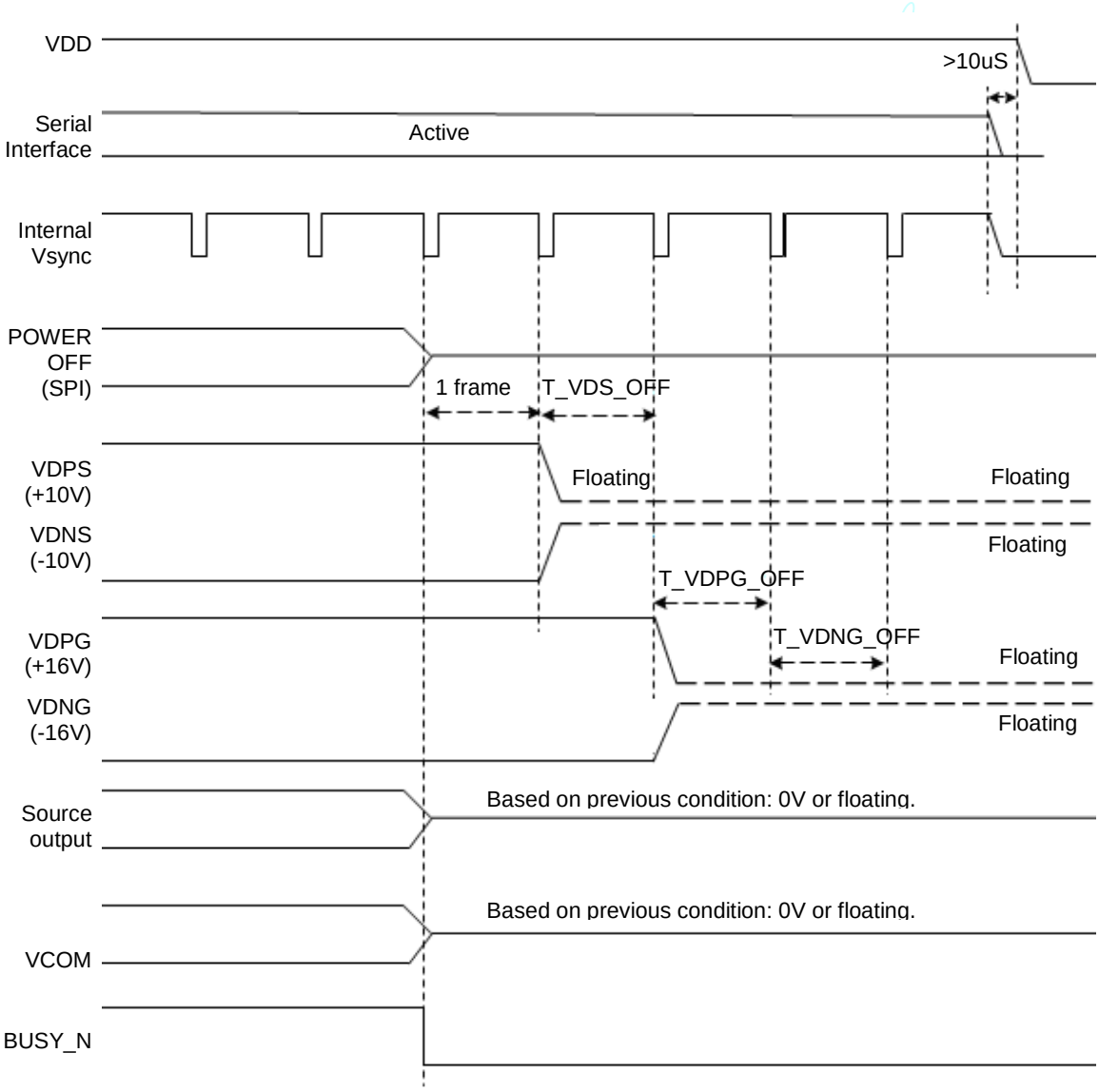


POWER MANAGEMENT

Power ON Sequence



Power OFF Sequence

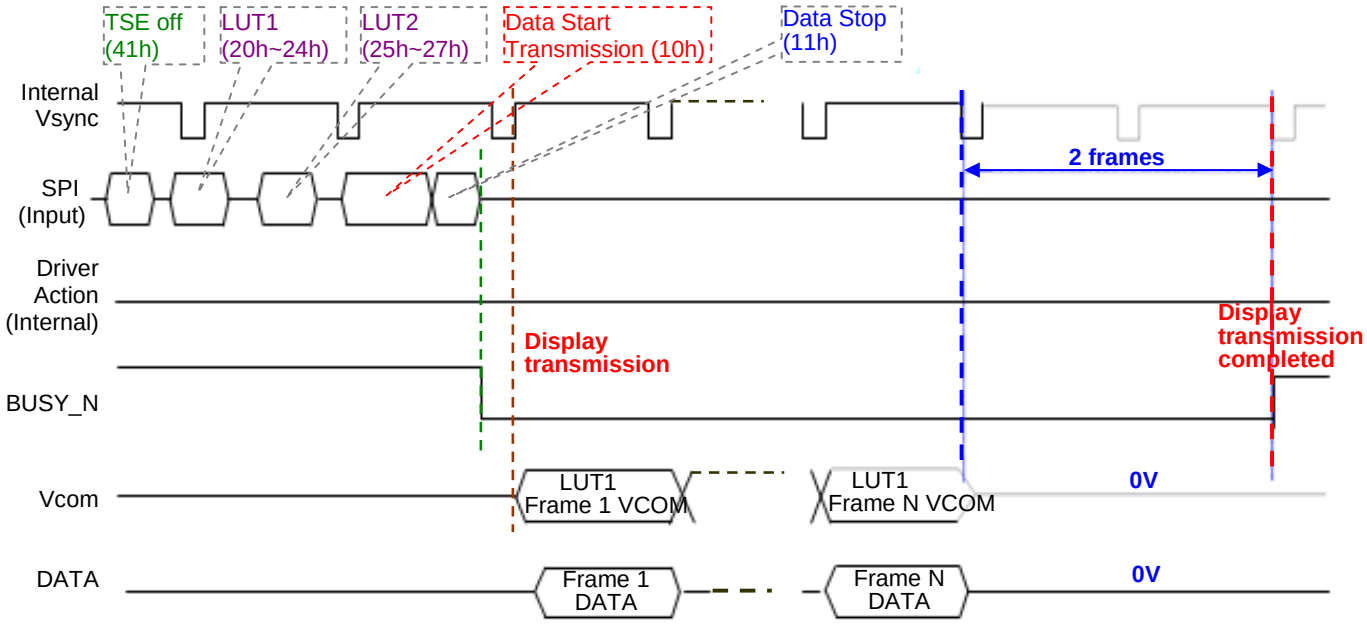


LUT (Lookup Table) Definition

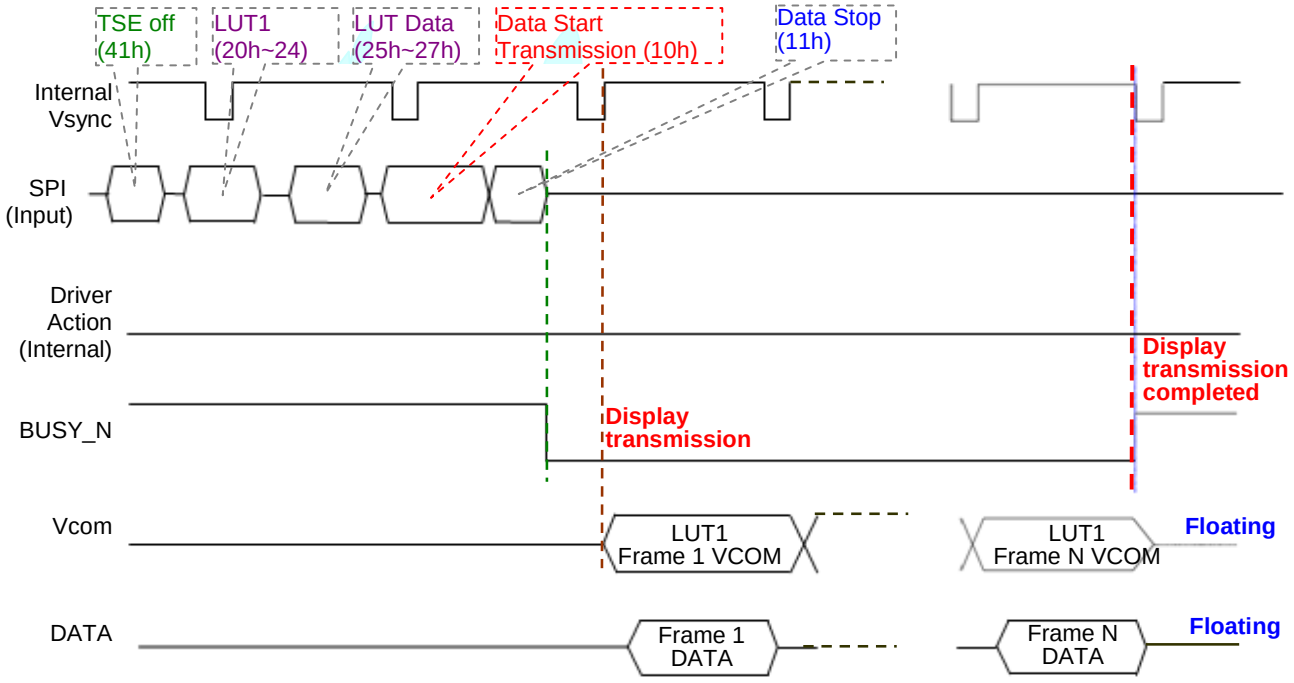
The LUT contains 10 temperature segments for application. And there are waveform, VCOM, XON, VDPS_L, VDNS_L, etc.
The total size of LUT is 25031 bytes.

Data Transmission Waveform

Example 1: LUT all states (10 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.

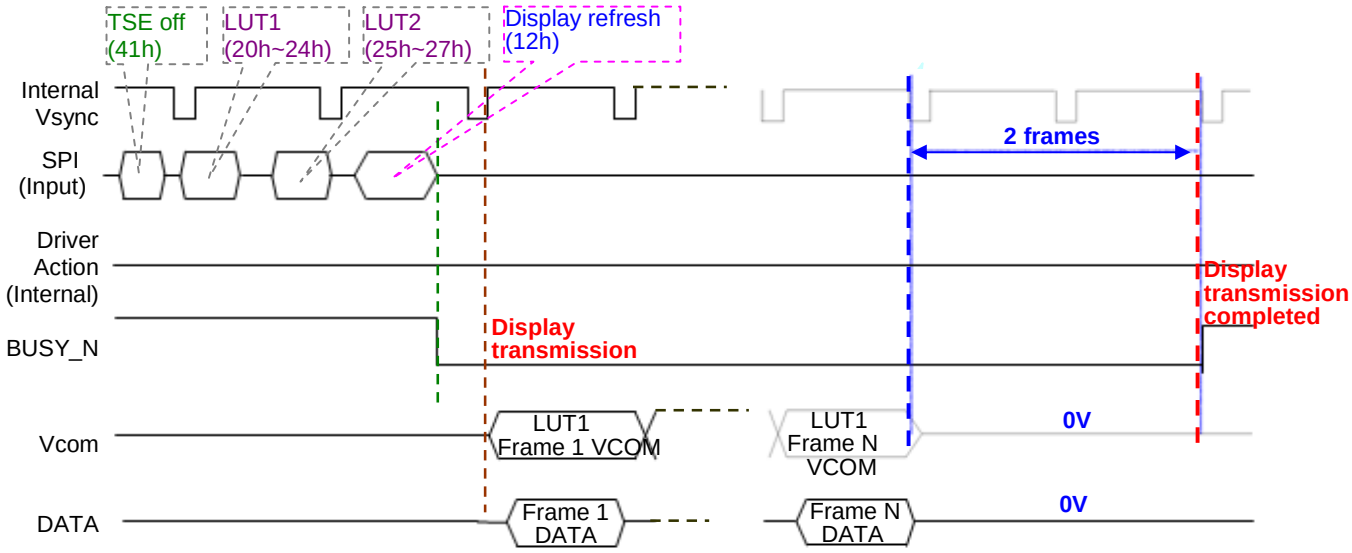


Example 2: While level selection in LUT is “11”, the driver will float VCOM and data.

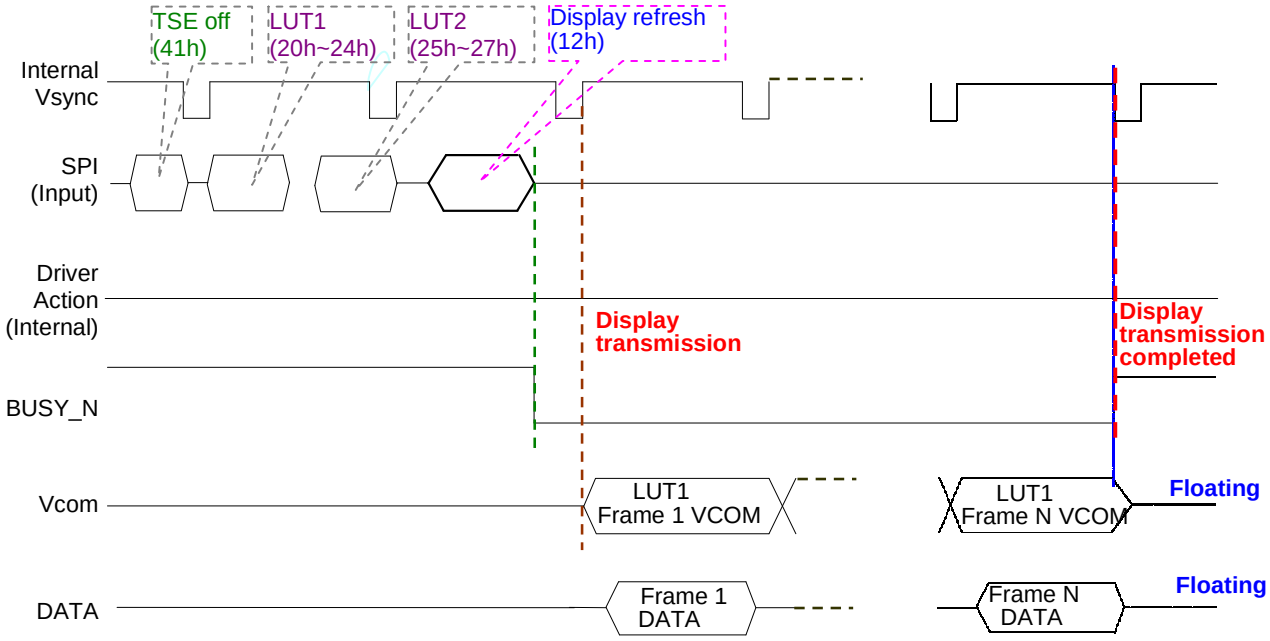


Display Refresh Waveform

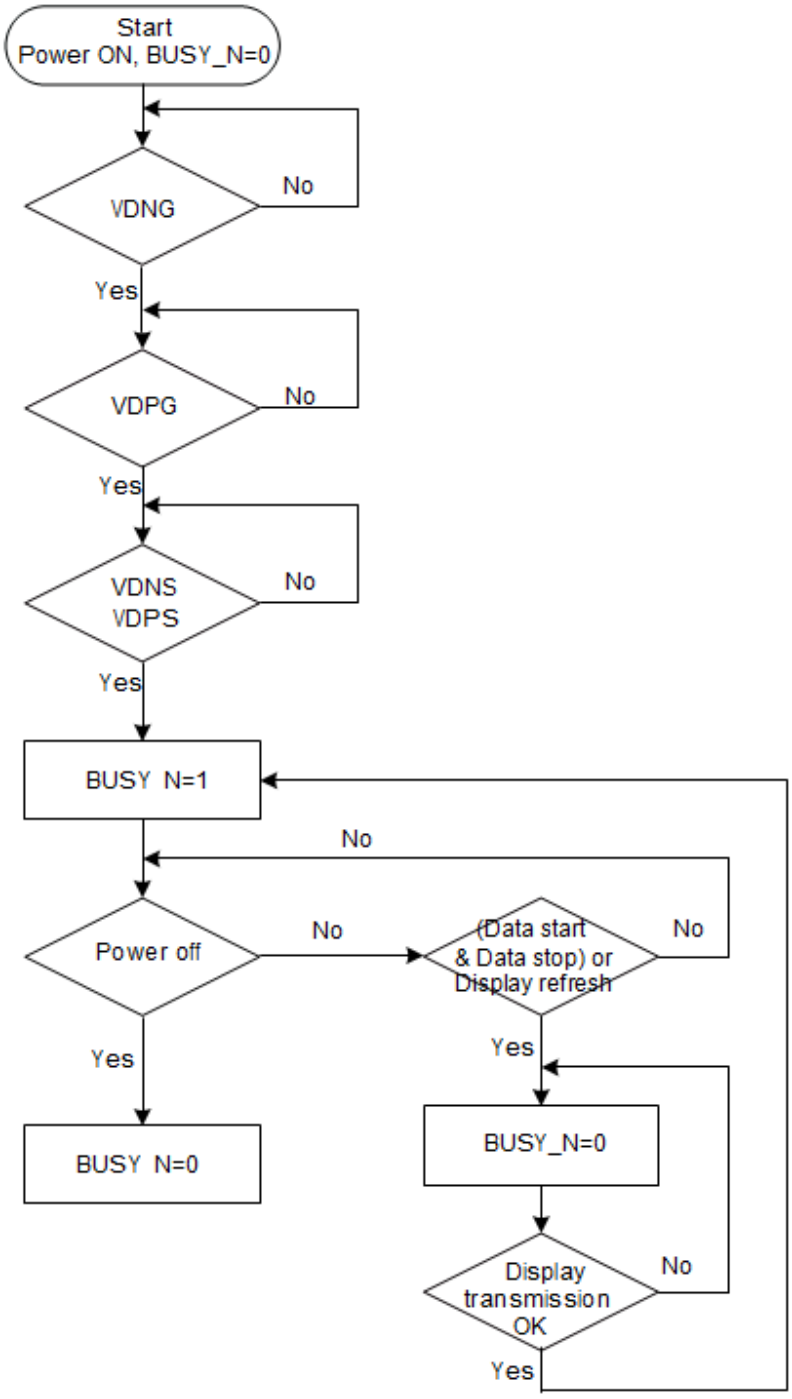
Example 1: LUT all states (10 states) complete or phase number=0, the driver will send 2 frames VCOM and data to 0 V.



Example2: While level selection in LUT is “11”, the driver will float VCOM and data.



BUSY_N Signal Flow Chart



BUSY_N Signal Flow Chart

ABSOLUTE MAXIMUM RATINGS

Signal	Item	Min	Max.	Unit
V_{DD}, V_{IO}, V_{DD1}, V_{PP}	Logic Supply voltage	- 0.3	+6.0	V
V_I	Digital input range	-0.3	V_{DDIO}+0.3	V
VDPG-VDNG	Supply range	VDNG-0.3	VDPG+0.3	V
Source				
VDPS	Analog supply voltage – positive	+16		V
VDNS	Analog supply voltage -- nagetive	-16		V
Gate				
V_{DPG}	Analog supply voltage – positive	-0.3	VDNG+42	V
V_{DNG}	Analog supply voltage -- nagetive	VDPG-42	0.3	V
I_{VDPG}	Input rush current for VDH	(TBD)	(TBD)	mA
I_{VDNG}	Input rush current for VDL	(TBD)	(TBD)	mA
T_{STG}	Storage temperature range	-55	+125	^{o}C

Warning:

If ICs are stressed beyond those listed above “absolute maximum ratings”, they may be permanently destroyed. These are stress ratings only, and functional operation of the device at these or any other condition beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

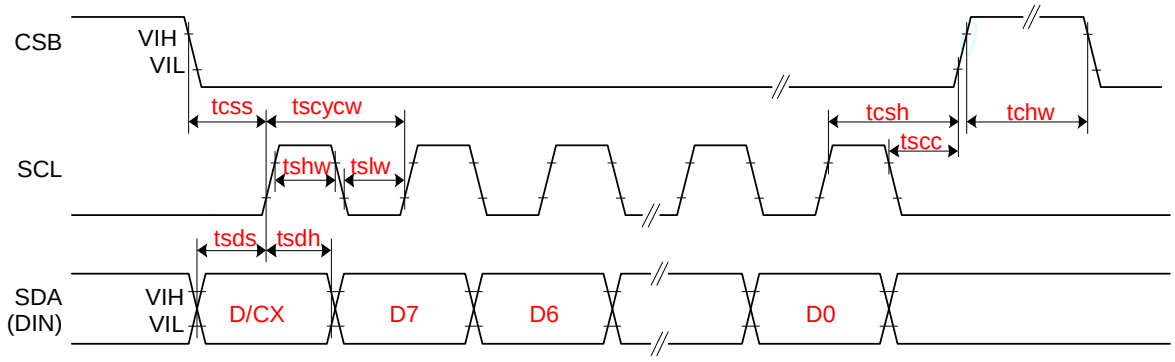
DC CHARACTERISTICS

DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
V_{IO}	IO supply voltage		2.3	3.3	3.6	V
V_{DD}	Supply voltage		2.3	3.3	3.6	V
$V_{DD}1$	DCDC driver supply voltage	DRVU, DRVD	2.3	3.3	3.6	V
V_{IL}	LOW Level input voltage	Digital input pins	GND	--	0.3xV_{DD}	V
V_{IH}	HIGH Level input voltage	Digital input pins	0.7xV_{IO}	--	V_{IO}	V
V_{OH}	HIGH Level output voltage	Digital input pins, I_{OH}=400uA	V_{IO}-0.4	--	--	V
V_{OHD}	HIGH Level output voltage	Digital input pins, I_{OH}=400uA, DRVD, DRVU	V_{DD}1-0.4	--	--	V
V_{OL}	LOW Level Output voltage	Digital input pins, I_{OL}=-400uA	GND	--	GND+0.4	V
I_{IN}	Input leakage current	Digital input pins except pull-up, pull-down pin	0	--	±1.0	uA
R_{IN}	Pull-up/down impedance			200		KΩ
I_{STVDD}	Digital stand-by current	all stopped (power off mode)	--	0	0.1	uV
I_{VDD}	Digital operating current		--	0.5	2.0	mV
I	IO stand-by current	all stopped (power off mode)		0.4	1.0	uV
I_{VIO}	IO operating current	No load		--	0.2	mA
$I_{STVDD}1$	DCDC stand-by current	all stopped (power off mode)		0	0.01	uA
$I_{VDD}1$	DCDC operating current	fdcdc=250kHz, No load		--	0.05	mA
		fdcdc=250kHz, External cap: 415pF, NMOS=340pF		0.5	1.0	
Top	Operating temperature		-30		85	°C

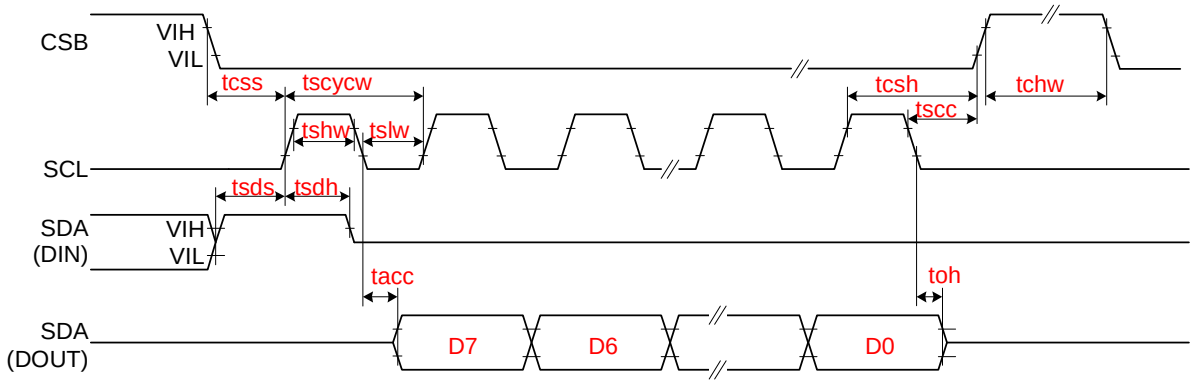
Note: TYP. and MAX. values are to be confirmed by design.

ANALOG DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VDPS	Supply Voltage	For source driver/VCOM		15		V
dVDPS	Supply voltage dev		-300	0	+300	mV
VDNS	Supply Voltage	For source driver/VCOM		-15		V
dVDNS	Supply voltage dev		-300	0	+300	mV
Idd	Analog Operating Current	No load,		TBD		mA
Vvd	Voltage Deviation of Outputs		--	±16	±35	mV
Vdr	Dynamic Range of Output		0.1	--	VDPS-0.1	V
VDPG-VDPG	Voltage Range of VGH - VGL		12		42	V
VDNG	VGL voltage Range	For gate driver	-20		-18	V
dVDNG	VGL Supply voltage dev		-400	0	+400	mV
VDPG	VGH voltage Range	For gate driver	20		22	V
dVDPG	VGH Supply voltage dev		-400	0	+400	mV
IstVDPG*	Positve HV Stand-by Current (power off mode)	Include VDH power With load	-	0	0.01	µA
IVDPG*	Positve HV Operating Current	Include VDH power With load all SD=L VCOM external resistor divider not included	-	0.7	1.1	mA
		Include VDH power With load all SD=H VCOM external resistor divider not included	-	0.8	1.2	mA
IstVDNG*	Negative HV Stand-by Current (power off mode)	Include VDPNS power With load	-	0	0.01	µA
IVDNG*	Negative HV Operating Current	Include VDL power With load all SD=L	-	0.8	1.2	mA
		Include VDL power With load all SD=H	-	0.9	1.3	mA
IstVINT1*	VINT1 Stand-by Current (power off mode)		-	0	0.01	µA
IVINT1*	VINT1 Operating Current		-	--	0.3	mA
Note: TYP. and MAX. values are to be confirmed by design.						

AC CHARACTERISTICS



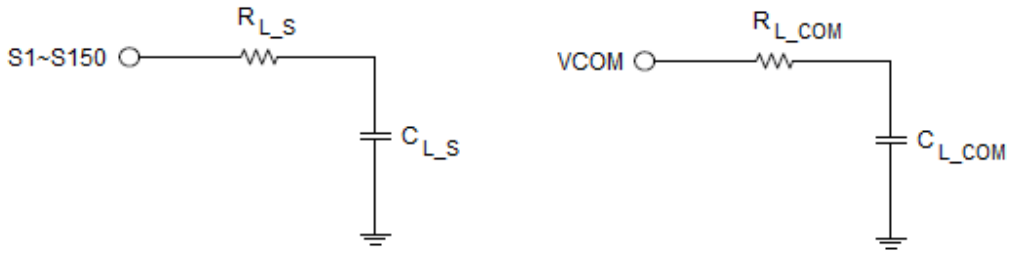
3-wire Serial Interface – Write



3-wire Serial Interface – Read

SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
SERIAL COMMUNICATION							
tCSS	CSB	Chip select setup time		60			ns
tCSH		Chip select hold time		65			ns
tSCC		Chip select setup time		20			ns
tCHW		Chip select setup time		40			ns
tSCYCW	SCL	Serial clock cycle (Write)		100			ns
tSHW		SCL “H” pulse width (Write)		35			ns
tSLW		SCL “L” pulse width (Write)		35			ns
tSCYCR		Serial clock cycle (Read)		150			ns
tSHR		SCL “H” pulse width (Read)		60			ns
tSLR		SCL “L” pulse width (Read)		60			ns
tSDS	SDA (DIN) (DOUT)	Data setup time		30			ns
tSDH		Data hold time		30			ns
tACC		Access time		10			ns
tOH		Output disable time		15			ns

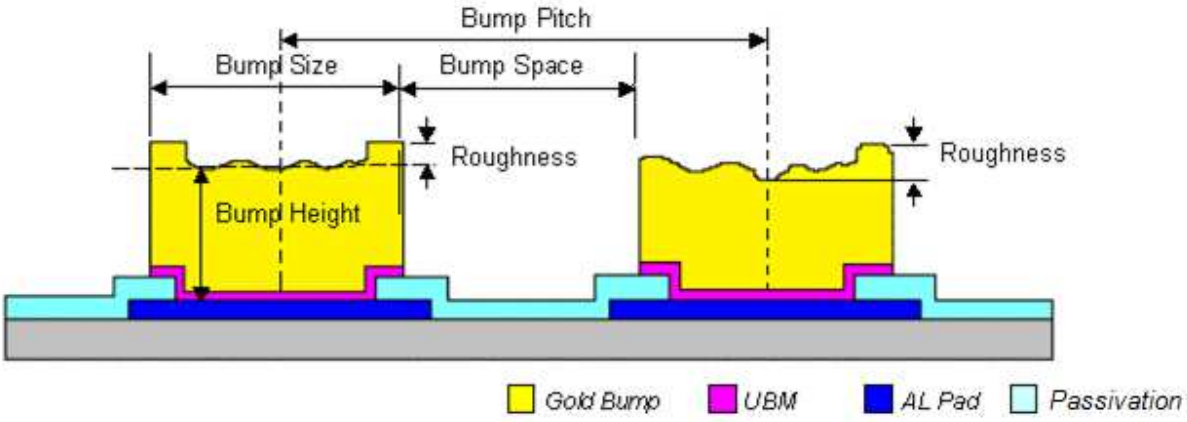
SYMBOL	SIGNAL			MIN.	TYP.	MAX.	UNIT
DRIVER							
trS		Source driver rise time	99% final value		5		uS
tFS		Source driver fall time			5		uS
trG		Gate driver rise time	99% final value		5		uS
tFG		Gate driver fall time			5		uS
trCOM		VCOM rise time	99% final value		1		mS
tFCOM		VCOM fall time			1		mS
RC LOADING							
R_{S_F}	Source driver	Source driver output loading (Fan-out)	Based on 6” panel		1962		Ω
C_{S_F}					5.7		pf
R_{S_A}		Source driver output loading (Active area)			1962		Ω
C_{S_A}					145.2		pf
R_{S_F}	Gate driver	Gate driver output loading (Fan-out)			7533		Ω
C_{S_F}					25.4		pf
R_{S_A}		Gate driver output loading (Active			2601		Ω
C_{S_A}					375.4		pf
R_{C_F}	VCOM	VCOM output loading (Fan-out)			5		Ω
C_{C_F}					0.6		pf
R_{C_A}		VCOM output loading (Active area)			83		Ω
C_{C_A}					30888		pf

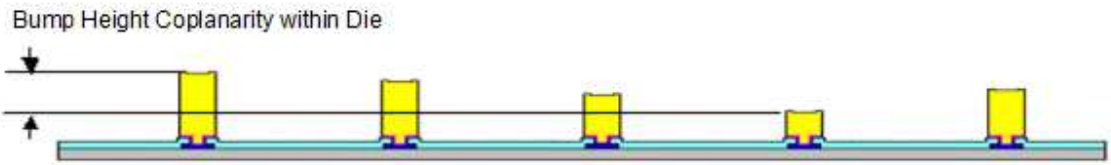


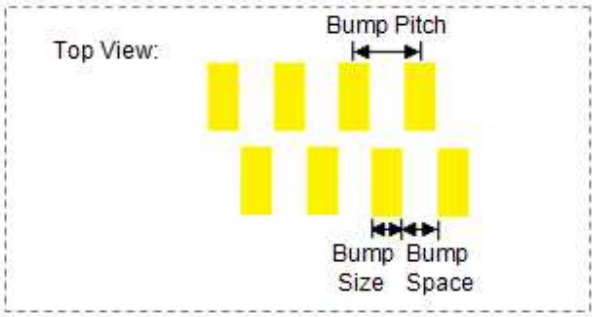
RC Loading

PHYSICAL DIMENSIONS

Die Size:	(17630 μM ± 40μM) x (1680 μM ± 40μM)
Die Thickness:	300 μM ± 20μM
Die TTV:	(D_{MAX} – D_{MIN}) within die ⩽ 2μM
Bump Height:	12 μM ± 3μM
	(H_{MAX} – H_{MIN}) within die ⩽ 2μM
Hardness:	65 Hv ± 15Hv
Bump Size:	12 μM x 100 μM ± 2μM
Bump Area:	1200 μM^2
Bump Pitch:	18 μM
Bump Gap:	15 μM ± 3μM
Shear:	⩾ 5g/Mil^2
Coordinate origin:	Chip center
Pad reference:	Pad center

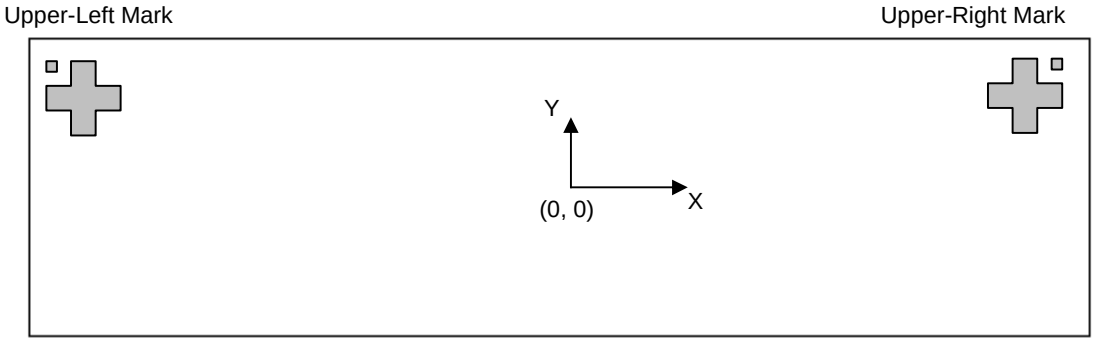




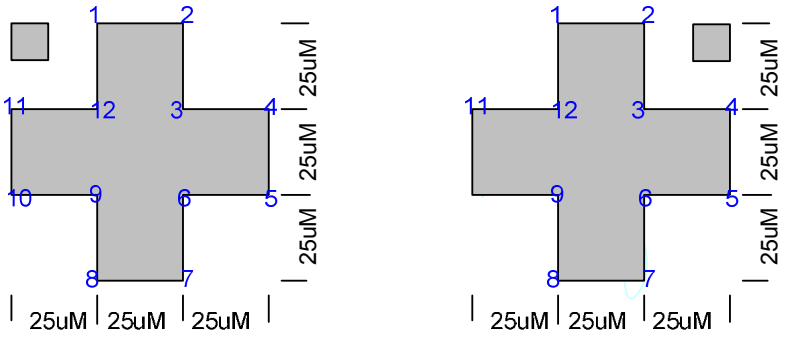


ALIGNMENT MARK INFORMATION

Location:



Shapes and Points:



Point Coordinates:

Point	Upper-Left Mark		Upper-Right Mark	
	X	Y	X	Y
Center	-8700	725	8700	725
1	-8712.5	762.5	8687.5	762.5
2	-8687.5	762.5	8712.5	762.5
3	-8687.5	737.5	8712.5	737.5
4	-8662.5	737.5	8737.5	737.5
5	-8662.5	712.5	8737.5	712.5
6	-8687.5	712.5	8712.5	712.5
7	-8687.5	687.5	8712.5	687.5
8	-8712.5	687.5	8687.5	687.5
9	-8712.5	712.5	8687.5	712.5
10	-8737.5	712.5	8662.5	712.5
11	-8737.5	737.5	8662.5	737.5
12	-8712.5	737.5	8687.5	737.5

PAD COORDINATES

No.	Name	X	Y	W	H
1	DUMMY	-8610	-755	40	50
2	VCOM	-8550	-755	40	50
3	VCOM	-8490	-755	40	50
4	VCOM	-8430	-755	40	50
5	VCOM	-8370	-755	40	50
6	VCOM	-8310	-755	40	50
7	VCOM	-8250	-755	40	50
8	VCOM	-8190	-755	40	50
9	VCOM	-8130	-755	40	50
10	PATH1	-8070	-755	40	50
11	VDM	-8010	-755	40	50
12	VDM	-7950	-755	40	50
13	VGL	-7890	-755	40	50
14	VGL	-7830	-755	40	50
15	VGL	-7770	-755	40	50
16	VGL	-7710	-755	40	50
17	VGL	-7650	-755	40	50
18	VGL	-7590	-755	40	50
19	VGL	-7530	-755	40	50
20	VGL	-7470	-755	40	50
21	VGL	-7410	-755	40	50
22	VGL	-7350	-755	40	50
23	VGL	-7290	-755	40	50
24	VGL	-7230	-755	40	50
25	VGL	-7170	-755	40	50
26	VGL	-7110	-755	40	50
27	VGL	-7050	-755	40	50
28	VGL	-6990	-755	40	50
29	GNDA	-6930	-755	40	50
30	VSL	-6870	-755	40	50
31	VSL	-6810	-755	40	50
32	VSL	-6750	-755	40	50
33	VSL	-6690	-755	40	50
34	VSL	-6630	-755	40	50
35	VSL	-6570	-755	40	50
36	VSL	-6510	-755	40	50
37	VSL	-6450	-755	40	50
38	VSL	-6390	-755	40	50
39	VSL	-6330	-755	40	50
40	GNDA	-6270	-755	40	50
42	VSL_LV	-6210	-755	40	50
41	VSL_LV	-6150	-755	40	50
43	VSL_LV	-6090	-755	40	50
44	VSL_LV	-6030	-755	40	50
45	VSL_LV	-5970	-755	40	50
46	VSL_LV	-5910	-755	40	50
47	VSL_LV	-5850	-755	40	50
48	VSL_LV	-5790	-755	40	50
49	VSL_LV	-5730	-755	40	50
50	VSL_LV	-5670	-755	40	50
51	GNDA	-5610	-755	40	50
52	VSL_LVX	-5550	-755	40	50
53	VSL_LVX	-5490	-755	40	50
54	VSL_LVX	-5430	-755	40	50
55	VSL_LVX	-5370	-755	40	50
56	VSL_LVX	-5310	-755	40	50
57	VSL_LVX	-5250	-755	40	50
58	VSL_LVX	-5190	-755	40	50

No.	Name	X	Y	W	H
59	VSL_LVX	-5130	-755	40	50
60	GNDA	-5070	-755	40	50
61	VGH	-5010	-755	40	50
62	VGH	-4950	-755	40	50
63	VGH	-4890	-755	40	50
64	VGH	-4830	-755	40	50
65	VGH	-4770	-755	40	50
66	VGH	-4710	-755	40	50
67	VGH	-4650	-755	40	50
68	VGH	-4590	-755	40	50
69	VGH	-4530	-755	40	50
70	VGH	-4470	-755	40	50
71	VGH	-4410	-755	40	50
72	VGH	-4350	-755	40	50
73	GNDA	-4290	-755	40	50
74	VSH	-4230	-755	40	50
75	VSH	-4170	-755	40	50
76	VSH	-4110	-755	40	50
77	VSH	-4050	-755	40	50
78	VSH	-3990	-755	40	50
79	VSH	-3930	-755	40	50
80	VSH	-3870	-755	40	50
81	VSH	-3810	-755	40	50
82	VSH	-3750	-755	40	50
83	VSH	-3690	-755	40	50
84	GNDA	-3630	-755	40	50
85	VSH_LV	-3570	-755	40	50
86	VSH_LV	-3510	-755	40	50
87	VSH_LV	-3450	-755	40	50
88	VSH_LV	-3390	-755	40	50
89	VSH_LV	-3330	-755	40	50
90	VSH_LV	-3270	-755	40	50
91	VSH_LV	-3210	-755	40	50
92	VSH_LV	-3150	-755	40	50
93	VSH_LV	-3090	-755	40	50
94	VSH_LV	-3030	-755	40	50
95	GNDA	-2970	-755	40	50
96	VSH_LVX	-2910	-755	40	50
97	VSH_LVX	-2850	-755	40	50
98	VSH_LVX	-2790	-755	40	50
99	VSH_LVX	-2730	-755	40	50
100	VSH_LVX	-2670	-755	40	50
101	VSH_LVX	-2610	-755	40	50
102	VSH_LVX	-2550	-755	40	50
103	VSH_LVX	-2490	-755	40	50
104	GNDA	-2430	-755	40	50
105	VDDD	-2370	-755	40	50
106	VDDD	-2310	-755	40	50
107	VDDD	-2250	-755	40	50
108	VDDD	-2190	-755	40	50
109	VDDD	-2130	-755	40	50
110	VDDD	-2070	-755	40	50
111	VDDDO	-2010	-755	40	50
112	VDDDO	-1950	-755	40	50
113	VDDDO	-1890	-755	40	50
114	VDDDO	-1830	-755	40	50
115	VDDDO	-1770	-755	40	50
116	VDDDO	-1710	-755	40	50

No.	Name	X	Y	W	H
117	GND	-1650	-755	40	50
118	VDM	-1590	-755	40	50
119	VDM	-1530	-755	40	50
120	GND	-1470	-755	40	50
121	GND	-1410	-755	40	50
122	GND	-1350	-755	40	50
123	GND	-1290	-755	40	50
124	GND	-1230	-755	40	50
125	GND	-1170	-755	40	50
126	GND	-1110	-755	40	50
127	GND	-1050	-755	40	50
128	GND	-990	-755	40	50
129	GND	-930	-755	40	50
130	GNDA	-870	-755	40	50
131	GNDA	-810	-755	40	50
132	GNDA	-750	-755	40	50
133	GNDA	-690	-755	40	50
134	GNDA	-630	-755	40	50
135	GNDA	-570	-755	40	50
136	GNDA	-510	-755	40	50
137	GNDA	-450	-755	40	50
138	GNDA	-390	-755	40	50
139	GNDA	-330	-755	40	50
140	GNDA	-270	-755	40	50
141	VDDA	-210	-755	40	50
142	VDDA	-150	-755	40	50
143	VDDA	-90	-755	40	50
144	VDDA	-30	-755	40	50
145	VDDA	30	-755	40	50
146	VDDA	90	-755	40	50
147	VDDA	150	-755	40	50
148	VDDA	210	-755	40	50
149	VDDA	270	-755	40	50
150	VDDA	330	-755	40	50
151	VDD	390	-755	40	50
152	VDD	450	-755	40	50
153	VDD	510	-755	40	50
154	VDD	570	-755	40	50
155	VDD	630	-755	40	50
156	VDD	690	-755	40	50
157	VDD	750	-755	40	50
158	VDD	810	-755	40	50
159	VDD	870	-755	40	50
160	VDD	930	-755	40	50
161	TEST1	990	-755	40	50
162	TEST2	1050	-755	40	50
163	VDDIO	1110	-755	40	50
164	VDDIO	1170	-755	40	50
165	VDDIO	1230	-755	40	50
166	VDDIO	1290	-755	40	50
167	TEST3	1350	-755	40	50
168	XCLK	1410	-755	40	50
169	XSTL	1470	-755	40	50
170	XOE	1530	-755	40	50
171	XLE	1590	-755	40	50
172	EDATA<0>	1650	-755	40	50
173	EDATA<1>	1710	-755	40	50
174	EDATA<2>	1770	-755	40	50
175	EDATA<3>	1830	-755	40	50
176	EDATA<4>	1890	-755	40	50

No.	Name	X	Y	W	H
177	EDATA<5>	1950	-755	40	50
178	EDATA<6>	2010	-755	40	50
179	EDATA<7>	2070	-755	40	50
180	GND	2130	-755	40	50
181	GCLK	2190	-755	40	50
182	STV	2250	-755	40	50
183	VDDIO	2310	-755	40	50
184	XON	2370	-755	40	50
185	DEN	2430	-755	40	50
186	GND	2490	-755	40	50
187	GND	2550	-755	40	50
188	FCSB	2610	-755	40	50
189	GND	2670	-755	40	50
190	FSCL	2730	-755	40	50
191	GND	2790	-755	40	50
192	FSDO	2850	-755	40	50
193	FSDI	2910	-755	40	50
194	SCL	2970	-755	40	50
195	SDA	3030	-755	40	50
196	GND	3090	-755	40	50
197	CSB	3150	-755	40	50
198	VDDIO	3210	-755	40	50
199	MFCSB	3270	-755	40	50
200	GND	3330	-755	40	50
201	DC	3390	-755	40	50
202	VDDIO	3450	-755	40	50
203	FMSDO	3510	-755	40	50
204	BUSY_N	3570	-755	40	50
205	GND	3630	-755	40	50
206	RST_N	3690	-755	40	50
207	TESTVDD	3750	-755	40	50
208	DUMMY	3810	-755	40	50
209	DUMMY	3870	-755	40	50
210	VDDIO	3930	-755	40	50
211	BS	3990	-755	40	50
212	GND	4050	-755	40	50
213	GND	4110	-755	40	50
214	VDD	4170	-755	40	50
215	VDD	4230	-755	40	50
216	VDDA	4290	-755	40	50
217	VDDA	4350	-755	40	50
218	TSDA	4410	-755	40	50
219	TSDA	4470	-755	40	50
220	TSCL	4530	-755	40	50
221	TSCL	4590	-755	40	50
222	GND	4650	-755	40	50
223	TEST4	4710	-755	40	50
224	GND	4770	-755	40	50
225	TEST5	4830	-755	40	50
226	GND	4890	-755	40	50
227	TEST6	4950	-755	40	50
228	GND	5010	-755	40	50
229	TEST7	5070	-755	40	50
230	TEST8	5130	-755	40	50
231	TEST9	5190	-755	40	50
232	TEST10	5250	-755	40	50
233	TEST11	5310	-755	40	50
234	TEST12	5370	-755	40	50
235	TEST13	5430	-755	40	50
236	TEST14	5490	-755	40	50

No.	Name	X	Y	W	H
237	TEST15	5550	-755	40	50
238	VCOMVS<0>	5610	-755	40	50
239	VCOMVS<1>	5670	-755	40	50
240	FSOURCE	5730	-755	40	50
241	FSOURCE	5790	-755	40	50
242	FSOURCE	5850	-755	40	50
243	VPPM	5910	-755	40	50
244	VPPM	5970	-755	40	50
245	VPPM	6030	-755	40	50
246	VPPM	6090	-755	40	50
247	VPPM	6150	-755	40	50
248	VPPM	6210	-755	40	50
249	VGH	6270	-755	40	50
250	VGH	6330	-755	40	50
251	VGH	6390	-755	40	50
252	VGH	6450	-755	40	50
253	VGH	6510	-755	40	50
254	VGH	6570	-755	40	50
255	VGH	6630	-755	40	50
256	VGH	6690	-755	40	50
257	VGL	6750	-755	40	50
258	VGL	6810	-755	40	50
259	VGL	6870	-755	40	50
260	VGL	6930	-755	40	50
261	VGL	6990	-755	40	50
262	VGL	7050	-755	40	50
263	VGL	7110	-755	40	50
264	GNDA	7170	-755	40	50
265	FB	7230	-755	40	50
266	FB	7290	-755	40	50
267	GNDA	7350	-755	40	50
268	RESE	7410	-755	40	50
269	RESE	7470	-755	40	50
270	GNDA	7530	-755	40	50
271	GDR	7590	-755	40	50
272	GDR	7650	-755	40	50
273	GDR	7710	-755	40	50
274	GDR	7770	-755	40	50
275	GDR	7830	-755	40	50
276	GDR	7890	-755	40	50
277	VDM	7950	-755	40	50
278	VDM	8010	-755	40	50
279	PATH1	8070	-755	40	50
280	VCOM	8130	-755	40	50
281	VCOM	8190	-755	40	50
282	VCOM	8250	-755	40	50
283	VCOM	8310	-755	40	50
284	VCOM	8370	-755	40	50
285	VCOM	8430	-755	40	50
286	VCOM	8490	-755	40	50
287	VCOM	8550	-755	40	50
288	DUMMY	8610	-755	40	50
289	DUMMY	8617	626	12	100
290	DUMMY	8602	751	12	100
291	G<0>	8587	626	12	100
292	G<2>	8572	751	12	100
293	G<4>	8557	626	12	100
294	G<6>	8542	751	12	100
295	G<8>	8527	626	12	100
296	G<10>	8512	751	12	100

No.	Name	X	Y	W	H
297	G<12>	8497	626	12	100
298	G<14>	8482	751	12	100
299	G<16>	8467	626	12	100
300	G<18>	8452	751	12	100
301	G<20>	8437	626	12	100
302	G<22>	8422	751	12	100
303	G<24>	8407	626	12	100
304	G<26>	8392	751	12	100
305	G<28>	8377	626	12	100
306	G<30>	8362	751	12	100
307	G<32>	8347	626	12	100
308	G<34>	8332	751	12	100
309	G<36>	8317	626	12	100
310	G<38>	8302	751	12	100
311	G<40>	8287	626	12	100
312	G<42>	8272	751	12	100
313	G<44>	8257	626	12	100
314	G<46>	8242	751	12	100
315	G<48>	8227	626	12	100
316	G<50>	8212	751	12	100
317	G<52>	8197	626	12	100
318	G<54>	8182	751	12	100
319	G<56>	8167	626	12	100
320	G<58>	8152	751	12	100
321	G<60>	8137	626	12	100
322	G<62>	8122	751	12	100
323	G<64>	8107	626	12	100
324	G<66>	8092	751	12	100
325	G<68>	8077	626	12	100
326	G<70>	8062	751	12	100
327	G<72>	8047	626	12	100
328	G<74>	8032	751	12	100
329	G<76>	8017	626	12	100
330	G<78>	8002	751	12	100
331	G<80>	7987	626	12	100
332	G<82>	7972	751	12	100
333	G<84>	7957	626	12	100
334	G<86>	7942	751	12	100
335	G<88>	7927	626	12	100
336	G<90>	7912	751	12	100
337	G<92>	7897	626	12	100
338	G<94>	7882	751	12	100
339	G<96>	7867	626	12	100
340	G<98>	7852	751	12	100
341	G<100>	7837	626	12	100
342	G<102>	7822	751	12	100
343	G<104>	7807	626	12	100
344	G<106>	7792	751	12	100
345	G<108>	7777	626	12	100
346	G<110>	7762	751	12	100
347	G<112>	7747	626	12	100
348	G<114>	7732	751	12	100
349	G<116>	7717	626	12	100
350	G<118>	7702	751	12	100
351	G<120>	7687	626	12	100
352	G<122>	7672	751	12	100
353	G<124>	7657	626	12	100
354	G<126>	7642	751	12	100
355	G<128>	7627	626	12	100
356	G<130>	7612	751	12	100

No.	Name	X	Y	W	H
357	G<132>	7597	626	12	100
358	G<134>	7582	751	12	100
359	G<136>	7567	626	12	100
360	G<138>	7552	751	12	100
361	G<140>	7537	626	12	100
362	G<142>	7522	751	12	100
363	G<144>	7507	626	12	100
364	G<146>	7492	751	12	100
365	G<148>	7477	626	12	100
366	G<150>	7462	751	12	100
367	G<152>	7447	626	12	100
368	G<154>	7432	751	12	100
369	G<156>	7417	626	12	100
370	G<158>	7402	751	12	100
371	G<160>	7387	626	12	100
372	G<162>	7372	751	12	100
373	G<164>	7357	626	12	100
374	G<166>	7342	751	12	100
375	G<168>	7327	626	12	100
376	G<170>	7312	751	12	100
377	G<172>	7297	626	12	100
378	G<174>	7282	751	12	100
379	G<176>	7267	626	12	100
380	G<178>	7252	751	12	100
381	G<180>	7237	626	12	100
382	G<182>	7222	751	12	100
383	G<184>	7207	626	12	100
384	G<186>	7192	751	12	100
385	G<188>	7177	626	12	100
386	G<190>	7162	751	12	100
387	G<192>	7147	626	12	100
388	G<194>	7132	751	12	100
389	G<196>	7117	626	12	100
390	G<198>	7102	751	12	100
391	G<200>	7087	626	12	100
392	G<202>	7072	751	12	100
393	G<204>	7057	626	12	100
394	G<206>	7042	751	12	100
395	G<208>	7027	626	12	100
396	G<210>	7012	751	12	100
397	G<212>	6997	626	12	100
398	G<214>	6982	751	12	100
399	G<216>	6967	626	12	100
400	G<218>	6952	751	12	100
401	G<220>	6937	626	12	100
402	G<222>	6922	751	12	100
403	G<224>	6907	626	12	100
404	G<226>	6892	751	12	100
405	G<228>	6877	626	12	100
406	G<230>	6862	751	12	100
407	G<232>	6847	626	12	100
408	G<234>	6832	751	12	100
409	G<236>	6817	626	12	100
410	G<238>	6802	751	12	100
411	G<240>	6787	626	12	100
412	G<242>	6772	751	12	100
413	G<244>	6757	626	12	100
414	G<246>	6742	751	12	100
415	G<248>	6727	626	12	100
416	G<250>	6712	751	12	100

No.	Name	X	Y	W	H
417	G<252>	6697	626	12	100
418	G<254>	6682	751	12	100
419	G<256>	6667	626	12	100
420	G<258>	6652	751	12	100
421	G<260>	6637	626	12	100
422	G<262>	6622	751	12	100
423	G<264>	6607	626	12	100
424	G<266>	6592	751	12	100
425	G<268>	6577	626	12	100
426	G<270>	6562	751	12	100
427	G<272>	6547	626	12	100
428	G<274>	6532	751	12	100
429	G<276>	6517	626	12	100
430	G<278>	6502	751	12	100
431	G<280>	6487	626	12	100
432	G<282>	6472	751	12	100
433	G<284>	6457	626	12	100
434	G<286>	6442	751	12	100
435	G<288>	6427	626	12	100
436	G<290>	6412	751	12	100
437	G<292>	6397	626	12	100
438	G<294>	6382	751	12	100
439	G<296>	6367	626	12	100
440	G<298>	6352	751	12	100
441	G<300>	6337	626	12	100
442	G<302>	6322	751	12	100
443	G<304>	6307	626	12	100
444	G<306>	6292	751	12	100
445	G<308>	6277	626	12	100
446	G<310>	6262	751	12	100
447	G<312>	6247	626	12	100
448	G<314>	6232	751	12	100
449	G<316>	6217	626	12	100
450	G<318>	6202	751	12	100
451	G<320>	6187	626	12	100
452	G<322>	6172	751	12	100
453	G<324>	6157	626	12	100
454	G<326>	6142	751	12	100
455	G<328>	6127	626	12	100
456	G<330>	6112	751	12	100
457	G<332>	6097	626	12	100
458	G<334>	6082	751	12	100
459	G<336>	6067	626	12	100
460	G<338>	6052	751	12	100
461	G<340>	6037	626	12	100
462	G<342>	6022	751	12	100
463	G<344>	6007	626	12	100
464	G<346>	5992	751	12	100
465	G<348>	5977	626	12	100
466	G<350>	5962	751	12	100
467	G<352>	5947	626	12	100
468	G<354>	5932	751	12	100
469	G<356>	5917	626	12	100
470	G<358>	5902	751	12	100
471	G<360>	5887	626	12	100
472	G<362>	5872	751	12	100
473	G<364>	5857	626	12	100
474	G<366>	5842	751	12	100
475	G<368>	5827	626	12	100
476	G<370>	5812	751	12	100

No.	Name	X	Y	W	H
477	G<372>	5797	626	12	100
478	G<374>	5782	751	12	100
479	G<376>	5767	626	12	100
480	G<378>	5752	751	12	100
481	G<380>	5737	626	12	100
482	G<382>	5722	751	12	100
483	G<384>	5707	626	12	100
484	G<386>	5692	751	12	100
485	G<388>	5677	626	12	100
486	G<390>	5662	751	12	100
487	G<392>	5647	626	12	100
488	G<394>	5632	751	12	100
489	G<396>	5617	626	12	100
490	G<398>	5602	751	12	100
491	G<400>	5587	626	12	100
492	G<402>	5572	751	12	100
493	G<404>	5557	626	12	100
494	G<406>	5542	751	12	100
495	G<408>	5527	626	12	100
496	G<410>	5512	751	12	100
497	G<412>	5497	626	12	100
498	G<414>	5482	751	12	100
499	G<416>	5467	626	12	100
500	G<418>	5452	751	12	100
501	G<420>	5437	626	12	100
502	G<422>	5422	751	12	100
503	G<424>	5407	626	12	100
504	G<426>	5392	751	12	100
505	G<428>	5377	626	12	100
506	G<430>	5362	751	12	100
507	G<432>	5347	626	12	100
508	G<434>	5332	751	12	100
509	G<436>	5317	626	12	100
510	G<438>	5302	751	12	100
511	G<440>	5287	626	12	100
512	G<442>	5272	751	12	100
513	G<444>	5257	626	12	100
514	G<446>	5242	751	12	100
515	G<448>	5227	626	12	100
516	G<450>	5212	751	12	100
517	G<452>	5197	626	12	100
518	G<454>	5182	751	12	100
519	G<456>	5167	626	12	100
520	G<458>	5152	751	12	100
521	G<460>	5137	626	12	100
522	G<462>	5122	751	12	100
523	G<464>	5107	626	12	100
524	G<466>	5092	751	12	100
525	G<468>	5077	626	12	100
526	G<470>	5062	751	12	100
527	G<472>	5047	626	12	100
528	G<474>	5032	751	12	100
529	G<476>	5017	626	12	100
530	G<478>	5002	751	12	100
531	DUMMY	4987	626	12	100
532	DUMMY	4830	751	12	100
533	VBD<0>	4815	626	12	100
534	S<0>	4800	751	12	100
535	S<1>	4785	626	12	100
536	S<2>	4770	751	12	100

No.	Name	X	Y	W	H
537	S<3>	4755	626	12	100
538	S<4>	4740	751	12	100
539	S<5>	4725	626	12	100
540	S<6>	4710	751	12	100
541	S<7>	4695	626	12	100
542	S<8>	4680	751	12	100
543	S<9>	4665	626	12	100
544	S<10>	4650	751	12	100
545	S<11>	4635	626	12	100
546	S<12>	4620	751	12	100
547	S<13>	4605	626	12	100
548	S<14>	4590	751	12	100
549	S<15>	4575	626	12	100
550	S<16>	4560	751	12	100
551	S<17>	4545	626	12	100
552	S<18>	4530	751	12	100
553	S<19>	4515	626	12	100
554	S<20>	4500	751	12	100
555	S<21>	4485	626	12	100
556	S<22>	4470	751	12	100
557	S<23>	4455	626	12	100
558	S<24>	4440	751	12	100
559	S<25>	4425	626	12	100
560	S<26>	4410	751	12	100
561	S<27>	4395	626	12	100
562	S<28>	4380	751	12	100
563	S<29>	4365	626	12	100
564	S<30>	4350	751	12	100
565	S<31>	4335	626	12	100
566	S<32>	4320	751	12	100
567	S<33>	4305	626	12	100
568	S<34>	4290	751	12	100
569	S<35>	4275	626	12	100
570	S<36>	4260	751	12	100
571	S<37>	4245	626	12	100
572	S<38>	4230	751	12	100
573	S<39>	4215	626	12	100
574	S<40>	4200	751	12	100
575	S<41>	4185	626	12	100
576	S<42>	4170	751	12	100
577	S<43>	4155	626	12	100
578	S<44>	4140	751	12	100
579	S<45>	4125	626	12	100
580	S<46>	4110	751	12	100
581	S<47>	4095	626	12	100
582	S<48>	4080	751	12	100
583	S<49>	4065	626	12	100
584	S<50>	4050	751	12	100
585	S<51>	4035	626	12	100
586	S<52>	4020	751	12	100
587	S<53>	4005	626	12	100
588	S<54>	3990	751	12	100
589	S<55>	3975	626	12	100
590	S<56>	3960	751	12	100
591	S<57>	3945	626	12	100
592	S<58>	3930	751	12	100
593	S<59>	3915	626	12	100
594	S<60>	3900	751	12	100
595	S<61>	3885	626	12	100
596	S<62>	3870	751	12	100

No.	Name	X	Y	W	H
597	S<63>	3855	626	12	100
598	S<64>	3840	751	12	100
599	S<65>	3825	626	12	100
600	S<66>	3810	751	12	100
601	S<67>	3795	626	12	100
602	S<68>	3780	751	12	100
603	S<69>	3765	626	12	100
604	S<70>	3750	751	12	100
605	S<71>	3735	626	12	100
606	S<72>	3720	751	12	100
607	S<73>	3705	626	12	100
608	S<74>	3690	751	12	100
609	S<75>	3675	626	12	100
610	S<76>	3660	751	12	100
611	S<77>	3645	626	12	100
612	S<78>	3630	751	12	100
613	S<79>	3615	626	12	100
614	S<80>	3600	751	12	100
615	S<81>	3585	626	12	100
616	S<82>	3570	751	12	100
617	S<83>	3555	626	12	100
618	S<84>	3540	751	12	100
619	S<85>	3525	626	12	100
620	S<86>	3510	751	12	100
621	S<87>	3495	626	12	100
622	S<88>	3480	751	12	100
623	S<89>	3465	626	12	100
624	S<90>	3450	751	12	100
625	S<91>	3435	626	12	100
626	S<92>	3420	751	12	100
627	S<93>	3405	626	12	100
628	S<94>	3390	751	12	100
629	S<95>	3375	626	12	100
630	S<96>	3360	751	12	100
631	S<97>	3345	626	12	100
632	S<98>	3330	751	12	100
633	S<99>	3315	626	12	100
634	S<100>	3300	751	12	100
635	S<101>	3285	626	12	100
636	S<102>	3270	751	12	100
637	S<103>	3255	626	12	100
638	S<104>	3240	751	12	100
639	S<105>	3225	626	12	100
640	S<106>	3210	751	12	100
641	S<107>	3195	626	12	100
642	S<108>	3180	751	12	100
643	S<109>	3165	626	12	100
644	S<110>	3150	751	12	100
645	S<111>	3135	626	12	100
646	S<112>	3120	751	12	100
647	S<113>	3105	626	12	100
648	S<114>	3090	751	12	100
649	S<115>	3075	626	12	100
650	S<116>	3060	751	12	100
651	S<117>	3045	626	12	100
652	S<118>	3030	751	12	100
653	S<119>	3015	626	12	100
654	S<120>	3000	751	12	100
655	S<121>	2985	626	12	100
656	S<122>	2970	751	12	100

No.	Name	X	Y	W	H
657	S<123>	2955	626	12	100
658	S<124>	2940	751	12	100
659	S<125>	2925	626	12	100
660	S<126>	2910	751	12	100
661	S<127>	2895	626	12	100
662	S<128>	2880	751	12	100
663	S<129>	2865	626	12	100
664	S<130>	2850	751	12	100
665	S<131>	2835	626	12	100
666	S<132>	2820	751	12	100
667	S<133>	2805	626	12	100
668	S<134>	2790	751	12	100
669	S<135>	2775	626	12	100
670	S<136>	2760	751	12	100
671	S<137>	2745	626	12	100
672	S<138>	2730	751	12	100
673	S<139>	2715	626	12	100
674	S<140>	2700	751	12	100
675	S<141>	2685	626	12	100
676	S<142>	2670	751	12	100
677	S<143>	2655	626	12	100
678	S<144>	2640	751	12	100
679	S<145>	2625	626	12	100
680	S<146>	2610	751	12	100
681	S<147>	2595	626	12	100
682	S<148>	2580	751	12	100
683	S<149>	2565	626	12	100
684	S<150>	2550	751	12	100
685	S<151>	2535	626	12	100
686	S<152>	2520	751	12	100
687	S<153>	2505	626	12	100
688	S<154>	2490	751	12	100
689	S<155>	2475	626	12	100
690	S<156>	2460	751	12	100
691	S<157>	2445	626	12	100
692	S<158>	2430	751	12	100
693	S<159>	2415	626	12	100
694	S<160>	2400	751	12	100
695	S<161>	2385	626	12	100
696	S<162>	2370	751	12	100
697	S<163>	2355	626	12	100
698	S<164>	2340	751	12	100
699	S<165>	2325	626	12	100
700	S<166>	2310	751	12	100
701	S<167>	2295	626	12	100
702	S<168>	2280	751	12	100
703	S<169>	2265	626	12	100
704	S<170>	2250	751	12	100
705	S<171>	2235	626	12	100
706	S<172>	2220	751	12	100
707	S<173>	2205	626	12	100
708	S<174>	2190	751	12	100
709	S<175>	2175	626	12	100
710	S<176>	2160	751	12	100
711	S<177>	2145	626	12	100
712	S<178>	2130	751	12	100
713	S<179>	2115	626	12	100
714	S<180>	2100	751	12	100
715	S<181>	2085	626	12	100
716	S<182>	2070	751	12	100

No.	Name	X	Y	W	H
717	S<183>	2055	626	12	100
718	S<184>	2040	751	12	100
719	S<185>	2025	626	12	100
720	S<186>	2010	751	12	100
721	S<187>	1995	626	12	100
722	S<188>	1980	751	12	100
723	S<189>	1965	626	12	100
724	S<190>	1950	751	12	100
725	S<191>	1935	626	12	100
726	S<192>	1920	751	12	100
727	S<193>	1905	626	12	100
728	S<194>	1890	751	12	100
729	S<195>	1875	626	12	100
730	S<196>	1860	751	12	100
731	S<197>	1845	626	12	100
732	S<198>	1830	751	12	100
733	S<199>	1815	626	12	100
734	S<200>	1800	751	12	100
735	S<201>	1785	626	12	100
736	S<202>	1770	751	12	100
737	S<203>	1755	626	12	100
738	S<204>	1740	751	12	100
739	S<205>	1725	626	12	100
740	S<206>	1710	751	12	100
741	S<207>	1695	626	12	100
742	S<208>	1680	751	12	100
743	S<209>	1665	626	12	100
744	S<210>	1650	751	12	100
745	S<211>	1635	626	12	100
746	S<212>	1620	751	12	100
747	S<213>	1605	626	12	100
748	S<214>	1590	751	12	100
749	S<215>	1575	626	12	100
750	S<216>	1560	751	12	100
751	S<217>	1545	626	12	100
752	S<218>	1530	751	12	100
753	S<219>	1515	626	12	100
754	S<220>	1500	751	12	100
755	S<221>	1485	626	12	100
756	S<222>	1470	751	12	100
757	S<223>	1455	626	12	100
758	S<224>	1440	751	12	100
759	S<225>	1425	626	12	100
760	S<226>	1410	751	12	100
761	S<227>	1395	626	12	100
762	S<228>	1380	751	12	100
763	S<229>	1365	626	12	100
764	S<230>	1350	751	12	100
765	S<231>	1335	626	12	100
766	S<232>	1320	751	12	100
767	S<233>	1305	626	12	100
768	S<234>	1290	751	12	100
769	S<235>	1275	626	12	100
770	S<236>	1260	751	12	100
771	S<237>	1245	626	12	100
772	S<238>	1230	751	12	100
773	S<239>	1215	626	12	100
774	S<240>	1200	751	12	100
775	S<241>	1185	626	12	100
776	S<242>	1170	751	12	100

No.	Name	X	Y	W	H
777	S<243>	1155	626	12	100
778	S<244>	1140	751	12	100
779	S<245>	1125	626	12	100
780	S<246>	1110	751	12	100
781	S<247>	1095	626	12	100
782	S<248>	1080	751	12	100
783	S<249>	1065	626	12	100
784	S<250>	1050	751	12	100
785	S<251>	1035	626	12	100
786	S<252>	1020	751	12	100
787	S<253>	1005	626	12	100
788	S<254>	990	751	12	100
789	S<255>	975	626	12	100
790	S<256>	960	751	12	100
791	S<257>	945	626	12	100
792	S<258>	930	751	12	100
793	S<259>	915	626	12	100
794	S<260>	900	751	12	100
795	S<261>	885	626	12	100
796	S<262>	870	751	12	100
797	S<263>	855	626	12	100
798	S<264>	840	751	12	100
799	S<265>	825	626	12	100
800	S<266>	810	751	12	100
801	S<267>	795	626	12	100
802	S<268>	780	751	12	100
803	S<269>	765	626	12	100
804	S<270>	750	751	12	100
805	S<271>	735	626	12	100
806	S<272>	720	751	12	100
807	S<273>	705	626	12	100
808	S<274>	690	751	12	100
809	S<275>	675	626	12	100
810	S<276>	660	751	12	100
811	S<277>	645	626	12	100
812	S<278>	630	751	12	100
813	S<279>	615	626	12	100
814	S<280>	600	751	12	100
815	S<281>	585	626	12	100
816	S<282>	570	751	12	100
817	S<283>	555	626	12	100
818	S<284>	540	751	12	100
819	S<285>	525	626	12	100
820	S<286>	510	751	12	100
821	S<287>	495	626	12	100
822	S<288>	480	751	12	100
823	S<289>	465	626	12	100
824	S<290>	450	751	12	100
825	S<291>	435	626	12	100
826	S<292>	420	751	12	100
827	S<293>	405	626	12	100
828	S<294>	390	751	12	100
829	S<295>	375	626	12	100
830	S<296>	360	751	12	100
831	S<297>	345	626	12	100
832	S<298>	330	751	12	100
833	S<299>	315	626	12	100
834	S<300>	300	751	12	100
835	S<301>	285	626	12	100
836	S<302>	270	751	12	100

No.	Name	X	Y	W	H
837	S<303>	255	626	12	100
838	S<304>	240	751	12	100
839	S<305>	225	626	12	100
840	S<306>	210	751	12	100
841	S<307>	195	626	12	100
842	S<308>	180	751	12	100
843	S<309>	165	626	12	100
844	S<310>	150	751	12	100
845	S<311>	135	626	12	100
846	S<312>	120	751	12	100
847	S<313>	105	626	12	100
848	S<314>	90	751	12	100
849	S<315>	75	626	12	100
850	S<316>	60	751	12	100
851	S<317>	45	626	12	100
852	S<318>	30	751	12	100
853	S<319>	15	626	12	100
854	S<320>	0	751	12	100
855	S<321>	-15	626	12	100
856	S<322>	-30	751	12	100
857	S<323>	-45	626	12	100
858	S<324>	-60	751	12	100
859	S<325>	-75	626	12	100
860	S<326>	-90	751	12	100
861	S<327>	-105	626	12	100
862	S<328>	-120	751	12	100
863	S<329>	-135	626	12	100
864	S<330>	-150	751	12	100
865	S<331>	-165	626	12	100
866	S<332>	-180	751	12	100
867	S<333>	-195	626	12	100
868	S<334>	-210	751	12	100
869	S<335>	-225	626	12	100
870	S<336>	-240	751	12	100
871	S<337>	-255	626	12	100
872	S<338>	-270	751	12	100
873	S<339>	-285	626	12	100
874	S<340>	-300	751	12	100
875	S<341>	-315	626	12	100
876	S<342>	-330	751	12	100
877	S<343>	-345	626	12	100
878	S<344>	-360	751	12	100
879	S<345>	-375	626	12	100
880	S<346>	-390	751	12	100
881	S<347>	-405	626	12	100
882	S<348>	-420	751	12	100
883	S<349>	-435	626	12	100
884	S<350>	-450	751	12	100
885	S<351>	-465	626	12	100
886	S<352>	-480	751	12	100
887	S<353>	-495	626	12	100
888	S<354>	-510	751	12	100
889	S<355>	-525	626	12	100
890	S<356>	-540	751	12	100
891	S<357>	-555	626	12	100
892	S<358>	-570	751	12	100
893	S<359>	-585	626	12	100
894	S<360>	-600	751	12	100
895	S<361>	-615	626	12	100
896	S<362>	-630	751	12	100

No.	Name	X	Y	W	H
897	S<363>	-645	626	12	100
898	S<364>	-660	751	12	100
899	S<365>	-675	626	12	100
900	S<366>	-690	751	12	100
901	S<367>	-705	626	12	100
902	S<368>	-720	751	12	100
903	S<369>	-735	626	12	100
904	S<370>	-750	751	12	100
905	S<371>	-765	626	12	100
906	S<372>	-780	751	12	100
907	S<373>	-795	626	12	100
908	S<374>	-810	751	12	100
909	S<375>	-825	626	12	100
910	S<376>	-840	751	12	100
911	S<377>	-855	626	12	100
912	S<378>	-870	751	12	100
913	S<379>	-885	626	12	100
914	S<380>	-900	751	12	100
915	S<381>	-915	626	12	100
916	S<382>	-930	751	12	100
917	S<383>	-945	626	12	100
918	S<384>	-960	751	12	100
919	S<385>	-975	626	12	100
920	S<386>	-990	751	12	100
921	S<387>	-1005	626	12	100
922	S<388>	-1020	751	12	100
923	S<389>	-1035	626	12	100
924	S<390>	-1050	751	12	100
925	S<391>	-1065	626	12	100
926	S<392>	-1080	751	12	100
927	S<393>	-1095	626	12	100
928	S<394>	-1110	751	12	100
929	S<395>	-1125	626	12	100
930	S<396>	-1140	751	12	100
931	S<397>	-1155	626	12	100
932	S<398>	-1170	751	12	100
933	S<399>	-1185	626	12	100
934	S<400>	-1200	751	12	100
935	S<401>	-1215	626	12	100
936	S<402>	-1230	751	12	100
937	S<403>	-1245	626	12	100
938	S<404>	-1260	751	12	100
939	S<405>	-1275	626	12	100
940	S<406>	-1290	751	12	100
941	S<407>	-1305	626	12	100
942	S<408>	-1320	751	12	100
943	S<409>	-1335	626	12	100
944	S<410>	-1350	751	12	100
945	S<411>	-1365	626	12	100
946	S<412>	-1380	751	12	100
947	S<413>	-1395	626	12	100
948	S<414>	-1410	751	12	100
949	S<415>	-1425	626	12	100
950	S<416>	-1440	751	12	100
951	S<417>	-1455	626	12	100
952	S<418>	-1470	751	12	100
953	S<419>	-1485	626	12	100
954	S<420>	-1500	751	12	100
955	S<421>	-1515	626	12	100
956	S<422>	-1530	751	12	100

No.	Name	X	Y	W	H
957	S<423>	-1545	626	12	100
958	S<424>	-1560	751	12	100
959	S<425>	-1575	626	12	100
960	S<426>	-1590	751	12	100
961	S<427>	-1605	626	12	100
962	S<428>	-1620	751	12	100
963	S<429>	-1635	626	12	100
964	S<430>	-1650	751	12	100
965	S<431>	-1665	626	12	100
966	S<432>	-1680	751	12	100
967	S<433>	-1695	626	12	100
968	S<434>	-1710	751	12	100
969	S<435>	-1725	626	12	100
970	S<436>	-1740	751	12	100
971	S<437>	-1755	626	12	100
972	S<438>	-1770	751	12	100
973	S<439>	-1785	626	12	100
974	S<440>	-1800	751	12	100
975	S<441>	-1815	626	12	100
976	S<442>	-1830	751	12	100
977	S<443>	-1845	626	12	100
978	S<444>	-1860	751	12	100
979	S<445>	-1875	626	12	100
980	S<446>	-1890	751	12	100
981	S<447>	-1905	626	12	100
982	S<448>	-1920	751	12	100
983	S<449>	-1935	626	12	100
984	S<450>	-1950	751	12	100
985	S<451>	-1965	626	12	100
986	S<452>	-1980	751	12	100
987	S<453>	-1995	626	12	100
988	S<454>	-2010	751	12	100
989	S<455>	-2025	626	12	100
990	S<456>	-2040	751	12	100
991	S<457>	-2055	626	12	100
992	S<458>	-2070	751	12	100
993	S<459>	-2085	626	12	100
994	S<460>	-2100	751	12	100
995	S<461>	-2115	626	12	100
996	S<462>	-2130	751	12	100
997	S<463>	-2145	626	12	100
998	S<464>	-2160	751	12	100
999	S<465>	-2175	26	12	100
1000	S<466>	-2190	751	12	100
1001	S<467>	-2205	626	12	100
1002	S<468>	-2220	751	12	100
1003	S<469>	-2235	626	12	100
1004	S<470>	-2250	751	12	100
1005	S<471>	-2265	626	12	100
1006	S<472>	-2280	751	12	100
1007	S<473>	-2295	626	12	100
1008	S<474>	-2310	751	12	100
1009	S<475>	-2325	626	12	100
1010	S<476>	-2340	751	12	100
1011	S<477>	-2355	626	12	100
1012	S<478>	-2370	751	12	100
1013	S<479>	-2385	626	12	100
1014	S<480>	-2400	751	12	100
1015	S<481>	-2415	626	12	100
1016	S<482>	-2430	751	12	100

No.	Name	X	Y	W	H
1017	S<483>	-2445	626	12	100
1018	S<484>	-2460	751	12	100
1019	S<485>	-2475	626	12	100
1020	S<486>	-2490	751	12	100
1021	S<487>	-2505	626	12	100
1022	S<488>	-2520	751	12	100
1023	S<489>	-2535	626	12	100
1024	S<490>	-2550	751	12	100
1025	S<491>	-2565	626	12	100
1026	S<492>	-2580	751	12	100
1027	S<493>	-2595	626	12	100
1028	S<494>	-2610	751	12	100
1029	S<495>	-2625	626	12	100
1030	S<496>	-2640	751	12	100
1031	S<497>	-2655	626	12	100
1032	S<498>	-2670	751	12	100
1033	S<499>	-2685	626	12	100
1034	S<500>	-2700	751	12	100
1035	S<501>	-2715	626	12	100
1036	S<502>	-2730	751	12	100
1037	S<503>	-2745	626	12	100
1038	S<504>	-2760	751	12	100
1039	S<505>	-2775	626	12	100
1040	S<506>	-2790	751	12	100
1041	S<507>	-2805	626	12	100
1042	S<508>	-2820	751	12	100
1043	S<509>	-2835	626	12	100
1044	S<510>	-2850	751	12	100
1045	S<511>	-2865	626	12	100
1046	S<512>	-2880	751	12	100
1047	S<513>	-2895	626	12	100
1048	S<514>	-2910	751	12	100
1049	S<515>	-2925	626	12	100
1050	S<516>	-2940	751	12	100
1051	S<517>	-2955	626	12	100
1052	S<518>	-2970	751	12	100
1053	S<519>	-2985	626	12	100
1054	S<520>	-3000	751	12	100
1055	S<521>	-3015	626	12	100
1056	S<522>	-3030	751	12	100
1057	S<523>	-3045	626	12	100
1058	S<524>	-3060	751	12	100
1059	S<525>	-3075	626	12	100
1060	S<526>	-3090	751	12	100
1061	S<527>	-3105	626	12	100
1062	S<528>	-3120	751	12	100
1063	S<529>	-3135	626	12	100
1064	S<530>	-3150	751	12	100
1065	S<531>	-3165	626	12	100
1066	S<532>	-3180	751	12	100
1067	S<533>	-3195	626	12	100
1068	S<534>	-3210	751	12	100
1069	S<535>	-3225	626	12	100
1070	S<536>	-3240	751	12	100
1071	S<537>	-3255	626	12	100
1072	S<538>	-3270	751	12	100
1073	S<539>	-3285	626	12	100
1074	S<540>	-3300	751	12	100
1075	S<541>	-3315	626	12	100
1076	S<542>	-3330	751	12	100

No.	Name	X	Y	W	H
1077	S<543>	-3345	626	12	100
1078	S<544>	-3360	751	12	100
1079	S<545>	-3375	626	12	100
1080	S<546>	-3390	751	12	100
1081	S<547>	-3405	626	12	100
1082	S<548>	-3420	751	12	100
1083	S<549>	-3435	626	12	100
1084	S<550>	-3450	751	12	100
1085	S<551>	-3465	626	12	100
1086	S<552>	-3480	751	12	100
1087	S<553>	-3495	626	12	100
1088	S<554>	-3510	751	12	100
1089	S<555>	-3525	626	12	100
1090	S<556>	-3540	751	12	100
1091	S<557>	-3555	626	12	100
1092	S<558>	-3570	751	12	100
1093	S<559>	-3585	626	12	100
1094	S<560>	-3600	751	12	100
1095	S<561>	-3615	626	12	100
1096	S<562>	-3630	751	12	100
1097	S<563>	-3645	626	12	100
1098	S<564>	-3660	751	12	100
1099	S<565>	-3675	626	12	100
1100	S<566>	-3690	751	12	100
1101	S<567>	-3705	626	12	100
1102	S<568>	-3720	751	12	100
1103	S<569>	-3735	626	12	100
1104	S<570>	-3750	751	12	100
1105	S<571>	-3765	626	12	100
1106	S<572>	-3780	751	12	100
1107	S<573>	-3795	626	12	100
1108	S<574>	-3810	751	12	100
1109	S<575>	-3825	626	12	100
1110	S<576>	-3840	751	12	100
1111	S<577>	-3855	626	12	100
1112	S<578>	-3870	751	12	100
1113	S<579>	-3885	626	12	100
1114	S<580>	-3900	751	12	100
1115	S<581>	-3915	626	12	100
1116	S<582>	-3930	751	12	100
1117	S<583>	-3945	626	12	100
1118	S<584>	-3960	751	12	100
1119	S<585>	-3975	626	12	100
1120	S<586>	-3990	751	12	100
1121	S<587>	-4005	626	12	100
1122	S<588>	-4020	751	12	100
1123	S<589>	-4035	626	12	100
1124	S<590>	-4050	751	12	100
1125	S<591>	-4065	626	12	100
1126	S<592>	-4080	751	12	100
1127	S<593>	-4095	626	12	100
1128	S<594>	-4110	751	12	100
1129	S<595>	-4125	626	12	100
1130	S<596>	-4140	751	12	100
1131	S<597>	-4155	626	12	100
1132	S<598>	-4170	751	12	100
1133	S<599>	-4185	626	12	100
1134	S<600>	-4200	751	12	100
1135	S<601>	-4215	626	12	100
1136	S<602>	-4230	751	12	100

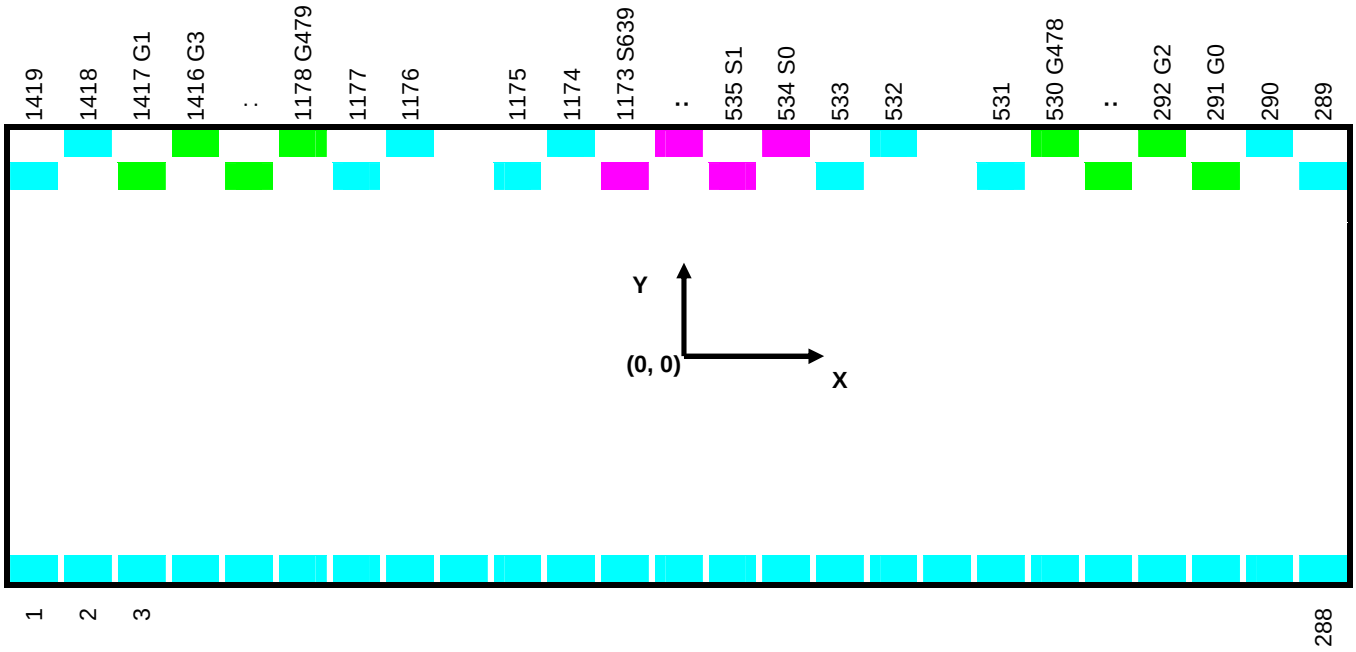
No.	Name	X	Y	W	H
1137	S<603>	-4245	626	12	100
1138	S<604>	-4260	751	12	100
1139	S<605>	-4275	626	12	100
1140	S<606>	-4290	751	12	100
1141	S<607>	-4305	626	12	100
1142	S<608>	-4320	751	12	100
1143	S<609>	-4335	626	12	100
1144	S<610>	-4350	751	12	100
1145	S<611>	-4365	626	12	100
1146	S<612>	-4380	751	12	100
1147	S<613>	-4395	626	12	100
1148	S<614>	-4410	751	12	100
1149	S<615>	-4425	626	12	100
1150	S<616>	-4440	751	12	100
1151	S<617>	-4455	626	12	100
1152	S<618>	-4470	751	12	100
1153	S<619>	-4485	626	12	100
1154	S<620>	-4500	751	12	100
1155	S<621>	-4515	626	12	100
1156	S<622>	-4530	751	12	100
1157	S<623>	-4545	626	12	100
1158	S<624>	-4560	751	12	100
1159	S<625>	-4575	626	12	100
1160	S<626>	-4590	751	12	100
1161	S<627>	-4605	626	12	100
1162	S<628>	-4620	751	12	100
1163	S<629>	-4635	626	12	100
1164	S<630>	-4650	751	12	100
1165	S<631>	-4665	626	12	100
1166	S<632>	-4680	751	12	100
1167	S<633>	-4695	626	12	100
1168	S<634>	-4710	751	12	100
1169	S<635>	-4725	626	12	100
1170	S<636>	-4740	751	12	100
1171	S<637>	-4755	626	12	100
1172	S<638>	-4770	751	12	100
1173	S<639>	-4785	626	12	100
1174	VBD<1>	-4800	751	12	100
1175	DUMMY	-4815	626	12	100
1176	DUMMY	-4972	751	12	100
1177	DUMMY	-4987	626	12	100
1178	G<479>	-5002	751	12	100
1179	G<477>	-5017	626	12	100
1180	G<475>	-5032	751	12	100
1181	G<473>	-5047	626	12	100
1182	G<471>	-5062	751	12	100
1183	G<469>	-5077	626	12	100
1184	G<467>	-5092	751	12	100
1185	G<465>	-5107	626	12	100
1186	G<463>	-5122	751	12	100
1187	G<461>	-5137	626	12	100
1188	G<459>	-5152	751	12	100
1189	G<457>	-5167	626	12	100
1190	G<455>	-5182	751	12	100
1191	G<453>	-5197	626	12	100
1192	G<451>	-5212	751	12	100
1193	G<449>	-5227	626	12	100
1194	G<447>	-5242	751	12	100
1195	G<445>	-5257	626	12	100
1196	G<443>	-5272	751	12	100

No.	Name	X	Y	W	H
1197	G<441>	-5287	626	12	100
1198	G<439>	-5302	751	12	100
1199	G<437>	-5317	626	12	100
1200	G<435>	-5332	751	12	100
1201	G<433>	-5347	626	12	100
1202	G<431>	-5362	751	12	100
1203	G<429>	-5377	626	12	100
1204	G<427>	-5392	751	12	100
1205	G<425>	-5407	626	12	100
1206	G<423>	-5422	751	12	100
1207	G<421>	-5437	626	12	100
1208	G<419>	-5452	751	12	100
1209	G<417>	-5467	626	12	100
1210	G<415>	-5482	751	12	100
1211	G<413>	-5497	626	12	100
1212	G<411>	-5512	751	12	100
1213	G<409>	-5527	626	12	100
1214	G<407>	-5542	751	12	100
1215	G<405>	-5557	626	12	100
1216	G<403>	-5572	751	12	100
1217	G<401>	-5587	626	12	100
1218	G<399>	-5602	751	12	100
1219	G<397>	-5617	626	12	100
1220	G<395>	-5632	751	12	100
1221	G<393>	-5647	626	12	100
1222	G<391>	-5662	751	12	100
1223	G<389>	-5677	626	12	100
1224	G<387>	-5692	751	12	100
1225	G<385>	-5707	626	12	100
1226	G<383>	-5722	751	12	100
1227	G<381>	-5737	626	12	100
1228	G<379>	-5752	751	12	100
1229	G<377>	-5767	626	12	100
1230	G<375>	-5782	751	12	100
1231	G<373>	-5797	626	12	100
1232	G<371>	-5812	751	12	100
1233	G<369>	-5827	626	12	100
1234	G<367>	-5842	751	12	100
1235	G<365>	-5857	626	12	100
1236	G<363>	-5872	751	12	100
1237	G<361>	-5887	626	12	100
1238	G<359>	-5902	751	12	100
1239	G<357>	-5917	626	12	100
1240	G<355>	-5932	751	12	100
1241	G<353>	-5947	626	12	100
1242	G<351>	-5962	751	12	100
1243	G<349>	-5977	626	12	100
1244	G<347>	-5992	751	12	100
1245	G<345>	-6007	626	12	100
1246	G<343>	-6022	751	12	100
1247	G<341>	-6037	626	12	100
1248	G<339>	-6052	751	12	100
1249	G<337>	-6067	626	12	100
1250	G<335>	-6082	751	12	100
1251	G<333>	-6097	626	12	100
1252	G<331>	-6112	751	12	100
1253	G<329>	-6127	626	12	100
1254	G<327>	-6142	751	12	100
1255	G<325>	-6157	626	12	100
1256	G<323>	-6172	751	12	100

No.	Name	X	Y	W	H
1257	G<321>	-6187	626	12	100
1258	G<319>	-6202	751	12	100
1259	G<317>	-6217	626	12	100
1260	G<315>	-6232	751	12	100
1261	G<313>	-6247	626	12	100
1262	G<311>	-6262	751	12	100
1263	G<309>	-6277	626	12	100
1264	G<307>	-6292	751	12	100
1265	G<305>	-6307	626	12	100
1266	G<303>	-6322	751	12	100
1267	G<301>	-6337	626	12	100
1268	G<299>	-6352	751	12	100
1269	G<297>	-6367	626	12	100
1270	G<295>	-6382	751	12	100
1271	G<293>	-6397	626	12	100
1272	G<291>	-6412	751	12	100
1273	G<289>	-6427	626	12	100
1274	G<287>	-6442	751	12	100
1275	G<285>	-6457	626	12	100
1276	G<283>	-6472	751	12	100
1277	G<281>	-6487	626	12	100
1278	G<279>	-6502	751	12	100
1279	G<277>	-6517	626	12	100
1280	G<275>	-6532	751	12	100
1281	G<273>	-6547	626	12	100
1282	G<271>	-6562	751	12	100
1283	G<269>	-6577	626	12	100
1284	G<267>	-6592	751	12	100
1285	G<265>	-6607	626	12	100
1286	G<263>	-6622	751	12	100
1287	G<261>	-6637	626	12	100
1288	G<259>	-6652	751	12	100
1289	G<257>	-6667	626	12	100
1290	G<255>	-6682	751	12	100
1291	G<253>	-6697	626	12	100
1292	G<251>	-6712	751	12	100
1293	G<249>	-6727	626	12	100
1294	G<247>	-6742	751	12	100
1295	G<245>	-6757	626	12	100
1296	G<243>	-6772	751	12	100
1297	G<241>	-6787	626	12	100
1298	G<239>	-6802	751	12	100
1299	G<237>	-6817	626	12	100
1300	G<235>	-6832	751	12	100
1301	G<233>	-6847	626	12	100
1302	G<231>	-6862	751	12	100
1303	G<229>	-6877	626	12	100
1304	G<227>	-6892	751	12	100
1305	G<225>	-6907	626	12	100
1306	G<223>	-6922	751	12	100
1307	G<221>	-6937	626	12	100
1308	G<219>	-6952	751	12	100
1309	G<217>	-6967	626	12	100
1310	G<215>	-6982	751	12	100
1311	G<213>	-6997	626	12	100
1312	G<211>	-7012	751	12	100
1313	G<209>	-7027	626	12	100
1314	G<207>	-7042	751	12	100
1315	G<205>	-7057	626	12	100
1316	G<203>	-7072	751	12	100

No.	Name	X	Y	W	H
1317	G<201>	-7087	626	12	100
1318	G<199>	-7102	751	12	100
1319	G<197>	-7117	626	12	100
1320	G<195>	-7132	751	12	100
1321	G<193>	-7147	626	12	100
1322	G<191>	-7162	751	12	100
1323	G<189>	-7177	626	12	100
1324	G<187>	-7192	751	12	100
1325	G<185>	-7207	626	12	100
1326	G<183>	-7222	751	12	100
1327	G<181>	-7237	626	12	100
1328	G<179>	-7252	751	12	100
1329	G<177>	-7267	626	12	100
1330	G<175>	-7282	751	12	100
1331	G<173>	-7297	626	12	100
1332	G<171>	-7312	751	12	100
1333	G<169>	-7327	626	12	100
1334	G<167>	-7342	751	12	100
1335	G<165>	-7357	626	12	100
1336	G<163>	-7372	751	12	100
1337	G<161>	-7387	626	12	100
1338	G<159>	-7402	751	12	100
1339	G<157>	-7417	626	12	100
1340	G<155>	-7432	751	12	100
1341	G<153>	-7447	626	12	100
1342	G<151>	-7462	751	12	100
1343	G<149>	-7477	626	12	100
1344	G<147>	-7492	751	12	100
1345	G<145>	-7507	626	12	100
1346	G<143>	-7522	751	12	100
1347	G<141>	-7537	626	12	100
1348	G<139>	-7552	751	12	100
1349	G<137>	-7567	626	12	100
1350	G<135>	-7582	751	12	100
1351	G<133>	-7597	626	12	100
1352	G<131>	-7612	751	12	100
1353	G<129>	-7627	626	12	100
1354	G<127>	-7642	751	12	100
1355	G<125>	-7657	626	12	100
1356	G<123>	-7672	751	12	100
1357	G<121>	-7687	626	12	100
1358	G<119>	-7702	751	12	100
1359	G<117>	-7717	626	12	100
1360	G<115>	-7732	751	12	100
1361	G<113>	-7747	626	12	100
1362	G<111>	-7762	751	12	100
1363	G<109>	-7777	626	12	100
1364	G<107>	-7792	751	12	100
1365	G<105>	-7807	626	12	100
1366	G<103>	-7822	751	12	100
1367	G<101>	-7837	626	12	100
1368	G<99>	-7852	751	12	100
1369	G<97>	-7867	626	12	100

No.	Name	X	Y	W	H
1370	G<95>	-7882	751	12	100
1371	G<93>	-7897	626	12	100
1372	G<91>	-7912	751	12	100
1373	G<89>	-7927	626	12	100
1374	G<87>	-7942	751	12	100
1375	G<85>	-7957	626	12	100
1376	G<83>	-7972	751	12	100
1377	G<81>	-7987	626	12	100
1378	G<79>	-8002	751	12	100
1379	G<77>	-8017	626	12	100
1380	G<75>	-8032	751	12	100
1381	G<73>	-8047	626	12	100
1382	G<71>	-8062	751	12	100
1383	G<69>	-8077	626	12	100
1384	G<67>	-8092	751	12	100
1385	G<65>	-8107	626	12	100
1386	G<63>	-8122	751	12	100
1387	G<61>	-8137	626	12	100
1388	G<59>	-8152	751	12	100
1389	G<57>	-8167	626	12	100
1390	G<55>	-8182	751	12	100
1391	G<53>	-8197	626	12	100
1392	G<51>	-8212	751	12	100
1393	G<49>	-8227	626	12	100
1394	G<47>	-8242	751	12	100
1395	G<45>	-8257	626	12	100
1396	G<43>	-8272	751	12	100
1397	G<41>	-8287	626	12	100
1398	G<39>	-8302	751	12	100
1399	G<37>	-8317	626	12	100
1400	G<35>	-8332	751	12	100
1401	G<33>	-8347	626	12	100
1402	G<31>	-8362	751	12	100
1403	G<29>	-8377	626	12	100
1404	G<27>	-8392	751	12	100
1405	G<25>	-8407	626	12	100
1406	G<23>	-8422	751	12	100
1407	G<21>	-8437	626	12	100
1408	G<19>	-8452	751	12	100
1409	G<17>	-8467	626	12	100
1410	G<15>	-8482	751	12	100
1411	G<13>	-8497	626	12	100
1412	G<11>	-8512	751	12	100
1413	G<9>	-8527	626	12	100
1414	G<7>	-8542	751	12	100
1415	G<5>	-8557	626	12	100
1416	G<3>	-8572	751	12	100
1417	G<1>	-8587	626	12	100
1418	DUMMY	-8602	751	12	100
1419	DUMMY	-8617	626	12	100


1419
1418
1417 G1
1416 G3
1178 G479
1177
1176
1175
1174
1173 S639
535 S1
534 S0
533
532
531
530 G478
292 G2
291 G0
290
289
Y
(0, 0)
X
1
2
3
288